

# Exhibit 16



US00RE43171E

(19) **United States**  
 (12) **Reissued Patent**  
**Chu**

(10) **Patent Number:** **US RE43,171 E**  
 (45) **Date of Reissued Patent:** **\*Feb. 7, 2012**

(54) **DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES**

(75) Inventor: **William W. Y. Chu**, Los Altos, CA (US)

(73) Assignee: **ACQIS LLC**, McKinney, TX (US)

(\*) Notice: This patent is subject to a terminal disclaimer.

(21) Appl. No.: **11/545,056**

(22) Filed: **Oct. 6, 2006**

#### Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **6,643,777**  
 Issued: **Nov. 4, 2003**  
 Appl. No.: **09/312,199**  
 Filed: **May 14, 1999**

(51) **Int. Cl.**  
**G06F 7/04** (2006.01)  
**G06F 11/30** (2006.01)

(52) **U.S. Cl.** ..... **726/2; 726/3; 726/4; 713/193**

(58) **Field of Classification Search** ..... **726/4, 5, 726/9, 20, 21, 2, 3; 713/183, 189, 192, 193, 713/194**

See application file for complete search history.

(56) **References Cited**

#### U.S. PATENT DOCUMENTS

3,996,585 A 12/1976 Hogan  
 4,141,068 A 2/1979 Mager et al.  
 4,228,496 A 10/1980 Katzman et al.  
 4,453,215 A 6/1984 Reid  
 4,623,964 A \* 11/1986 Getz et al. .... 705/1  
 4,670,837 A 6/1987 Sheets  
 4,680,674 A 7/1987 Moore  
 4,700,362 A 10/1987 Todd et al.

4,760,276 A 7/1988 Lethellier  
 4,769,764 A 9/1988 Levanon  
 4,791,524 A 12/1988 Teigen et al.  
 4,799,258 A 1/1989 Davies  
 4,872,091 A 10/1989 Maniwa et al.  
 4,890,282 A 12/1989 Lambert et al.  
 4,918,572 A 4/1990 Tarver et al.  
 4,939,735 A 7/1990 Fredericks et al.  
 5,056,141 A \* 10/1991 Dyke ..... 340/5.27  
 5,086,499 A 2/1992 Mutone  
 5,103,446 A 4/1992 Fischer  
 5,187,645 A 2/1993 Spalding et al.  
 5,191,581 A 3/1993 Woodbury et al.  
 5,251,097 A 10/1993 Simmons et al.

(Continued)

#### FOREIGN PATENT DOCUMENTS

EP 722138 A1 7/1996

(Continued)

#### OTHER PUBLICATIONS

PC Magazine Online. "Think Modular" (Jun. 10, 1997).

(Continued)

*Primary Examiner* — Eleni Shiferaw

*Assistant Examiner* — Ali S Abyaneh

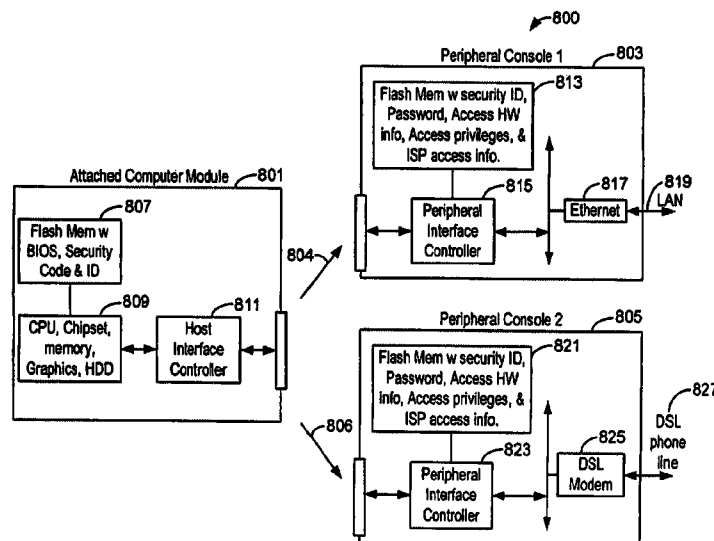
(74) *Attorney, Agent, or Firm* — Cooley LLP

(57)

#### ABSTRACT

A security method for an attached computer module in a computer system. The security method reads a security identification number in an attached computer module and compares it to a security identification number in a console, which houses the attached computer module. Based upon a relationship between these numbers, a security status is selected. The security status determines the security level of operating the computer system.

**53 Claims, 14 Drawing Sheets**



## US RE43,171 E

Page 2

U.S. PATENT DOCUMENTS			
5,278,509 A	1/1994	Haynes et al.	5,933,609 A 8/1999 Walker et al.
5,278,730 A	1/1994	Kikinis	5,941,965 A 8/1999 Moroz
5,282,247 A	1/1994	McLean et al.	5,948,047 A 9/1999 Jenkins et al.
5,293,487 A	3/1994	Russo et al.	5,960,213 A 9/1999 Wilson
5,293,497 A	3/1994	Free	5,965,957 A 10/1999 Bourgeois
5,311,397 A	5/1994	Harshberger et al.	5,968,144 A 10/1999 Walker et al.
5,317,441 A	5/1994	Sidman	5,971,804 A 10/1999 Gallagher et al.
5,317,477 A	5/1994	Gillett	5,974,486 A 10/1999 Siddappa
5,319,771 A	6/1994	Takeda	5,977,989 A 11/1999 Lee et al.
5,325,517 A	6/1994	Baker et al.	5,978,821 A 11/1999 Freeny
5,331,509 A	7/1994	Kikinis	5,978,919 A 11/1999 Doi et al.
5,339,408 A	8/1994	Bruckert et al.	5,982,363 A 11/1999 Naift
5,355,391 A	10/1994	Horowitz et al.	5,982,614 A 11/1999 Reid
5,428,806 A	6/1995	Pocrass	5,991,163 A 11/1999 Marconi et al.
5,430,607 A	7/1995	Smith	5,991,844 A 11/1999 Khosrowpour
5,432,939 A	7/1995	Blackledge, Jr. et al.	5,999,952 A * 12/1999 Jenkins et al. .... 708/100
5,436,857 A	7/1995	Nelson et al.	6,002,442 A 12/1999 Li et al.
5,436,902 A	7/1995	McNamara et al.	6,003,105 A 12/1999 Vicard
5,463,742 A	10/1995	Kobayashi	6,006,243 A 12/1999 Karidis
5,519,843 A	5/1996	Moran et al.	6,009,488 A 12/1999 Kavipurapu
5,533,125 A	7/1996	Bensimon et al.	6,011,546 A 1/2000 Bertram
5,537,544 A	7/1996	Morisawa et al.	6,012,145 A * 1/2000 Mathers et al. .... 726/17
5,539,616 A	7/1996	Kikinis	6,016,252 A 1/2000 Pignolet et al.
5,546,463 A	8/1996	Caputo et al.	6,025,989 A 2/2000 Ayd et al.
5,550,710 A	8/1996	Rahamim et al.	6,028,643 A 2/2000 Jordan et al.
5,550,861 A	8/1996	Chan et al.	6,029,183 A 2/2000 Jenkins et al.
5,552,776 A	9/1996	Wade et al.	6,038,621 A 3/2000 Gale et al.
5,572,441 A	11/1996	Boie	6,040,792 A 3/2000 Watson et al.
5,577,205 A	11/1996	Hwang et al.	6,046,571 A 4/2000 Bovio et al.
5,578,940 A	11/1996	Dillon	6,049,823 A 4/2000 Hwang
5,588,850 A	12/1996	Pan et al.	6,052,513 A 4/2000 McLaren
5,590,377 A	12/1996	Smith	6,069,615 A 5/2000 Abraham et al.
5,600,800 A	2/1997	Kikinis et al.	6,070,211 A 5/2000 Neal
5,603,044 A	2/1997	Annapareddy et al.	6,070,214 A 5/2000 Ahern
5,606,717 A	2/1997	Farmwald et al.	6,078,503 A 6/2000 Gallagher et al.
5,608,608 A	3/1997	Flint et al.	6,088,224 A 7/2000 Gallagher et al.
5,623,637 A	4/1997	Jones et al.	6,088,620 A 7/2000 Ninomiya et al.
5,630,057 A	5/1997	Hait	6,088,752 A 7/2000 Ahern
5,638,521 A	6/1997	Buchala et al.	6,091,737 A 7/2000 Hong et al.
5,640,302 A	6/1997	Kikinis	6,104,921 A 8/2000 Cosley et al.
5,648,762 A *	7/1997	Ichimura et al. .... 726/34	6,145,085 A 11/2000 Tran et al.
5,659,773 A	8/1997	Huynh et al.	6,157,534 A 12/2000 Gallagher et al.
5,663,661 A	9/1997	Dillon et al.	6,161,524 A 12/2000 Akbarian et al.
5,673,172 A	9/1997	Hastings et al.	6,163,464 A 12/2000 Ishibashi et al.
5,673,174 A	9/1997	Hamirani	6,175,490 B1 1/2001 Papa et al.
5,680,126 A	10/1997	Kikinis	6,188,602 B1 2/2001 Alexander et al.
5,680,536 A	10/1997	Tyuluman	6,202,169 B1 3/2001 Razzaghe-Ashrafi et al.
5,689,654 A	11/1997	Kikinis	6,208,522 B1 3/2001 Manweiler et al.
5,708,840 A	1/1998	Kikinis et al.	6,216,185 B1 * 4/2001 Chu .... 710/303
5,721,837 A	2/1998	Kikinis	6,256,689 B1 7/2001 Khosrowpour
5,721,842 A	2/1998	Beasley et al.	6,256,691 B1 7/2001 Moroz et al.
5,724,591 A	3/1998	Hara et al.	6,260,155 B1 7/2001 Dellacona
5,737,194 A	4/1998	Hopkins et al.	6,266,539 B1 7/2001 Pardo
5,737,524 A	4/1998	Cohen et al.	6,289,376 B1 9/2001 Taylor et al.
5,745,733 A	4/1998	Robinson	6,297,955 B1 10/2001 Frank, Jr. et al.
5,751,711 A	5/1998	Sakaue	6,301,637 B1 10/2001 Krull et al.
5,752,080 A	5/1998	Ryan	6,304,895 B1 10/2001 Schneider et al.
5,764,924 A	6/1998	Hong	6,311,268 B1 10/2001 Chu
5,774,703 A	6/1998	Weiss et al.	6,311,287 B1 10/2001 Dischler et al.
5,774,704 A	6/1998	Williams	6,314,522 B1 11/2001 Chu et al.
5,795,228 A	8/1998	Trumbull	6,317,329 B1 11/2001 Dowdy et al.
5,802,391 A	9/1998	Hwang	6,321,335 B1 11/2001 Chu
5,805,903 A	9/1998	Elkhoury	6,324,605 B1 11/2001 Rafferty et al.
5,809,262 A	9/1998	Potter	6,325,636 B1 12/2001 Hipp et al.
5,809,538 A	9/1998	Pollmann	6,332,180 B1 12/2001 Kauffman et al.
5,815,681 A	9/1998	Kikinis	6,345,330 B2 2/2002 Chu
5,819,050 A	10/1998	Boehling et al.	6,366,951 B1 4/2002 Schmidt
5,826,048 A	10/1998	Dempsey et al.	6,378,009 B1 4/2002 Pinkston, II et al.
5,838,932 A	11/1998	Alzien	6,381,602 B1 * 4/2002 Shoroff et al. .... 707/9
5,848,249 A	12/1998	Garbus	6,393,561 B1 * 5/2002 Hagiwara et al. .... 713/100
5,859,669 A	1/1999	Prentice	6,401,124 B1 6/2002 Yang et al.
5,862,350 A	1/1999	Coulson	6,411,506 B1 6/2002 Hipp et al.
5,862,381 A	1/1999	Advani et al.	6,425,033 B1 7/2002 Conway
5,878,211 A *	3/1999	Delagrange et al. .... 726/34	6,452,789 B1 9/2002 Pallotti et al.
5,884,049 A	3/1999	Atkinson	6,452,790 B1 9/2002 Chu et al.
5,884,053 A	3/1999	Clouser	6,453,344 B1 9/2002 Ellsworth
5,907,566 A *	5/1999	Benson et al. .... 714/798	6,496,361 B2 * 12/2002 Kim et al. .... 361/683
5,930,110 A	7/1999	Nishigaki et al.	6,498,361 B1 12/2002 Osann, Jr.
			6,549,966 B1 4/2003 Dickens et al.

## US RE43,171 E

Page 3

6,564,274	B1	5/2003	Heath et al.
6,567,877	B1	5/2003	Lewis et al.
6,578,103	B1	6/2003	Hill
6,581,125	B1	6/2003	Lange
6,606,253	B2	8/2003	Jackson et al.
6,643,777	B1	11/2003	Chu
6,664,377	B1	12/2003	Xu
6,715,100	B1	3/2004	Hwang
6,718,415	B1	4/2004	Chu
6,725,317	B1	4/2004	Bouchier et al.
6,742,068	B2	5/2004	Gallagher et al.
6,747,878	B1	6/2004	Hipp et al.
6,757,748	B1	6/2004	Hipp
6,948,047	B2	9/2005	Maruska et al.
6,985,967	B1	1/2006	Hipp
7,017,001	B2	3/2006	Hill et al.
7,020,735	B2	3/2006	Kikinis
7,099,981	B2	8/2006	Chu
7,146,446	B2	12/2006	Chu
7,328,297	B2	2/2008	Chu
7,339,786	B2	3/2008	Bottom et al.
7,363,415	B2	4/2008	Chu
7,363,416	B2	4/2008	Chu
7,376,779	B2	5/2008	Chu
RE41,076	E	1/2010	Chu
RE41,092	E	1/2010	Chu
7,676,624	B2	3/2010	Chu
RE41,294	E	4/2010	Chu
7,818,487	B2	10/2010	Chu
RE41,961	E	11/2010	Chu
2001/0011312	A1	8/2001	Chu
2005/0182882	A1	8/2005	Chu
2009/0157939	A1	6/2009	Chu
2010/0174844	A1	7/2010	Chu

## FOREIGN PATENT DOCUMENTS

JP	6-289953	10/1994
JP	6-289956	10/1994
JP	7-64672	3/1995
JP	7-84675	3/1995
WO	WO 92/18924	10/1992
WO	WO 94/00097	1/1994
WO	WO 94/00970	1/1994
WO	WO 95/13640	5/1995
WO	W097/00481	1/1997
WO	WO 97/05618	2/1997

## OTHER PUBLICATIONS

Spang. "Component House: Design Technology for 'PCs in a snap'—NeoSystems Offers Building Blocks". Techweb, 2 pp. (Apr. 21, 1997) No. 732:Channel Assembly.

Faegre, et al. "Unisys' Best-Kept Secret Is An Operating System Built For Distributed Business Applications." Core Technologies / CTOS Revealed, 6 pp. (Dec. 1994).

Boyd-Merritt. "Upgradable-PC Effort Takes Divergent Paths." EE Times Headline News, 3 pp. (1997). <http://techweb.cmp.com/eet/news/97/949new/effort.html>.

Berst. "Hope For The Modular PCs We all Really Want." ZDNet, 3 pp. (Dec. 5, 1997). [http://www.zdnet.com/anchordesk/story/story\\_1504.html](http://www.zdnet.com/anchordesk/story/story_1504.html).

Liquorman. "Convergent Technologies Had This Idea." Talkback to Jesse Berst, 1 pp. (Dec. 5, 1997).

U.S. Appl. No. 12/322,858, filed Feb. 5, 2009, Chu.

Part 3: Carrier sense multiple access with collision detertion (CSMA/CD) access method and physical layer specifications, IEEE Standard 802.3z, The Institute of Electrical and Electronics Engineers, Inc., Jul. 1998, 1262 pages.

Microsoft Cluster Service Center, "MSCS Basics", <<<http://www.networks.com/mscsbasics.htm>>>, downloaded from web on Feb. 7, 2005, 6 pgs.

Intel Corporation, Intel 82559 Fast Ethernet Controller, [retrieved on Mar. 14, 2011], Retrieved from the Internet: <URL: <http://www.intel.com/design/network/products/lan/controllers/82559.htm>>, 1 page.

Gruener, J., "Vendors Pack in More Servers," PC Week, vol. 14, No. 1, Mar. 17, 1997, 2 pages.

Microsoft Press Computer User's Dictionary, pp. 82 and 232, Kim Fryer ed., Microsoft Press, 1998, 5 pages.

IBM Thinkpad Product Information Guide, IBM PC Company, Apr. 28, 1998, 26 pages.

The American Heritage Dictionary, pp. 536, 607 and 770, Dell Publishing, 1994, 5 pages.

The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Ed., p. 1236, The Institute of Electrical and Electronics Engineers, Inc., 1993, 3 pages.

Microsoft Press Computer Dictionary, Third Ed., pp. 96, 313, and 355, Kim Fryer ed., Microsoft Press, 1997, 5 pages.

IBM Dictionary of Computing, Tenth Ed., pp. 139, 439, 480 and 629, George McDaniel ed., McGraw-Hill, Inc., Aug. 1993, 16 pages.

IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Ed., pp. 703, 704, 856 and 1064, The Institute of Electrical and Electronics Engineers, Inc., 2000, 13 pages.

Microsoft Press Computer Dictionary, Second Edition, pp. 82, 92, 93 and 260, Alice Smith ed., Microsoft Press, 1994, 13 pages.

Microsoft Press Computer User's Dictionary, pp. 232, 262, and 275, Kim Fryer ed., Microsoft Press, 1998, 12 pages.

Feibel, W., Encyclopedia of Networking, Third Edition, p. 265, The Network Press, 2000, 4 pages.

IEEE Standard for a High Performance Serial Bus, IEEE Std 1394-1995, The Institute of Electrical and Electronics Engineers, Inc., 1996, 392 pages.

RLX System 324 Hardware Installation Guide, RLX Technologies, Inc., 2001, 80 pages.

RLX System 324 Platform Guide: RLX Linux Web Server, RLX Technologies, Inc., 2001, 73 pages.

RLX System 324 Technical Guide: RLX Control Tower SNMP Implementation, RLX Technologies, 2001, 32 pages.

RLX System 324 Technical Guide: RLX Control Tower SNMP Implementation, Supplementary Document, Draft, RLX Technologies, May 26, 2001, 48 pages.

RLX System 324 Technical Guide: RLX Control Tower Backup/Restore, Draft, RLX Technologies, May 18, 2001, 8 pages.

"RocketLogix Passive I/O Board Topology," RocketLogix, Inc., Revision 6, May 24, 2000, 1 page.

"RocketLogix Switched I/O Board Topology," RocketLogix, Inc., Revision 6, May 24, 2000, 1 page.

"Redefining Server Economics—Take Control," RLX Technologies, 2001, 2 pages.

RLX Technologies Presentation, RLX Technologies, Inc., Apr. 27, 2001, 44 pages.

"Engineering Design Proposal for RocketLogix, Inc.," Anigma, Inc., Apr. 19, 2000, 35 pages.

RLX Blade, RLX Technologies, 2001, 2 pages.

"RLX System 324 Technical Guide: RLX Red Hat Installation," RLX Technologies, Inc., 2001, 22 pages.

"Firmware Interface Specification, Orbiter 1680, Orbiter 3360," Anigma, Inc., Aug. 17, 2000, 16 pages.

Board Specifications for DataModule Board, DataStation Backplane, DataStation Front Bezel, and BaseStation Backplane, Rev. E, Anigma, Inc., Mar. 2, 2000, 5 pages.

"Logical Management Process," RocketLogix, Rev. 5, Apr. 5, 2000, 1 page.

Eversys Corporation Business Plan, Eversys Corporation, Mar. 21, 1997, 53 pages.

System 8000 Web Product Brief, Eversys Corporation, [retrieved on Oct. 22, 2009], Retrieved from the Internet: <URL: <http://www.web.archive.org/web/1997052509465/www.eversys.com/Products/S8000/Brief/Index/htm>>, 6 pages.

Nicholls, T., "9800 First level design," White Cross Systems Limited, Mar. 26, 1997, 26 pages.

Nicholls, T., "9800 System Architecture," White Cross Systems Limited, Mar. 27, 1997, 28 pages.

Feakes, L., "Fast Ethernet Switch Card Design Specification," Revision 4.00, White Cross Systems Limited, Jul. 27, 2010, 23 pages.

Phillips, J., "9800 Power System Backplane Design Specification," Revision 1.00, White Cross Systems Limited, Oct. 22, 1997, 11 pages.

Phillips, J., "9800 Auxiliary PSU Design Specification," Revision 1.00, White Cross Systems Limited, Oct. 27, 1997, 13 pages.

## US RE43,171 E

Page 4

- "Narus and Whitecross Join Forces to Deliver Comprehensive Usage Pattern Analysis Applications for IP Service Providers," Press Release, Palo Alto, CA, Mar. 27, 2000, 4 pages.
- "P6000 Fault-Tolerant Multiprocessor Application Server," Powerstation Technologies, Inc., 1996, 3 pages.
- Network Engines P6000 System Guide, Revision C, Network Engines, Inc., Jul. 1998, 89 pages.
- Network Engines P6000EXP System Guide, Revision A, Network Engines, Inc., Jan. 1998, 106 pages.
- Powerstation Technologies P6000 System Guide, Powerstation Technologies, Inc., 1996, 65 pages.
- Network Engines™ SBC2000ST Reference Guide, Rev. A, Network Engines, Inc., Oct. 1998, 178 pages.
- Network Engines™ SBC2000S Reference Guide, Rev. 1.0, Network Engines, Inc., Sep. 1998, 156 pages.
- Network Engines™ SBC2000 User's Manual, Rev. 1.0, Network Engines, Inc., Jul. 1998, 140 pages.
- Network Engines™ SBC1000 User's Manual, Rev. E Draft, Network Engines, Inc., Jun. 1998, 75 pages.
- Pentium Processor™ Network Engines™ P586 Guide, Issue 0.0.20 Preliminary, Network Engines, Inc., Nov. 10, 1997, 58 pages.
- "PTI Fault Tolerant System Working Document Specification," Rev 0, Feb. 26, 1996, 2 pages.
- Network Engines Network, Network Engines, Inc., Jun. 22, 1999, 20 pages.
- "HMU—586 Card Guide (Mustang) Pentium PCI," Issue 0.0.14 Preliminary, HM Systems, Inc., Nov. 18, 1996, 57 pages.
- "TLD Queries Complete Call Detail Record Database with WhiteCross Data Exploration Server," Data Mining Product Reviews, Feb. 2000, 1 page.
- "WhiteCross Data Exploration Announces ExplorationSTUDIO™," Press Release, New York, NY, Sep. 2, 1999, 2 pages.
- "WhiteCross Introduces 'World's Most Powerful Exploration Warehouse System,'" Press Release, New York, NY, Sep. 2, 1999, 2 pages.
- Charlesworth, I., "Technology Audit, Data Exploration Server," Butler Group, Sep. 1999, 8 pages.
- Groom, P., "WhiteCross 9800 pre-release configuration details and USA Pricing Information," WhiteCross Systems Limited, Nov. 3, 1998, 4 pages.
- "Kognitio—Infrastructure Partners," Retrieved from the Internet on Sep. 8, 2010, Retrieved at URL: [www.kognitio.com/partners/infrastructure.php](http://www.kognitio.com/partners/infrastructure.php), 2 pages.
- RocketLogix Presentation, RocketLogix, Inc., Apr. 6, 2000, 84 pages.
- "Expanding the Reach of the Internet with a New Breed of Web Server Appliances," RocketLogix, Inc., May 2000, 10 pages.
- Radigan, J., "A Solution to the Power Shortage?" CFO.com, Jan. 17, 2001, [online] Retrieved from the Internet on Dec. 14, 2007, Retrieved at URL: [www.cfo.com/article.cfm/2991376?f=singlepage](http://www.cfo.com/article.cfm/2991376?f=singlepage), 3 pages.
- Goldman, A., "ISP Profiles: RLX Technologies," ISP-Planet, May 17, 2001, retrieved from the Internet on Jul. 26, 2001, Retrieved at URL: [www.isp-planet.com/profiles/2001/rlx.html](http://www.isp-planet.com/profiles/2001/rlx.html), 3 pages.
- Rosencrance, L., "IBM agrees to resell RLX high-density servers," Computerworld, May 8, 2001, retrieved from the Internet on Jul. 25, 2001, Retrieved at URL: [www.itworld.com/Comp/1362/CWD010508STO60353/pfindex.html](http://www.itworld.com/Comp/1362/CWD010508STO60353/pfindex.html), 3 pages.
- "ChatCom, Inc. Announces Results for the Dec. 31, 1996 Quarter," ChatCom, Inc., Press Release, Feb. 12, 1997, 2 pages.
- "ChatCom Defines Specification for Future Consolidated Server Products, RAINSTM Concept to Accelerate the Adoption of Consolidated Servers," ChatCom, Inc., Press Release, Mar. 31, 1997, 2 pages.
- "ChatCom, Inc. Announces PentiumPro/200 MHz Server Module, Server Module Offers Scalability and High Availability for File Server Environments," ChatCom, Inc., Press Release, Mar. 24, 1997, 3 pages.
- "ChatCom Strengthens Sales Management Team, Three New Sales Directors to Address Growing Demand for ChatCom's Chat-terBox™," ChatCom, Inc., Press Release, Mar. 18, 1997, 2 pages.
- "ChatCom Announces Major Push into International Markets, Significant International Sales Opportunities for ChatCom's Consolidated Server Technology," ChatCom, Inc., Press Release, Mar. 18, 1997, 2 pages.
- "ChatCom Receives Product Award From LAN Times Magazine, Consolidated Server Product Comparison Puts ChatCom on Top," ChatCom, Inc., Press Release, Feb. 20, 1997, 2 pages.
- "Astro Sciences Corporation Shareholders Elect Two New Directors, and Vote to Change Corporate Name to ChatCom, Inc.," Astro Sciences Corporation, Press Release, Feb. 12, 1996, 2 pages.
- "ChatCom, Inc., (Formerly Astro Sciences Corporation) Trades Under New Symbol—NASDAQ/NMS: Chat," ChatCom, Inc., New Release, Feb. 22, 1996, 1 page.
- "ChatCom Names James B. Mariner President/CEO," ChatCom, Inc., Press Release, Mar. 7, 1996, 2 pages.
- "ChatCom Selected as Partner in Anixter Race '96 Program and Completes First Part of Financing," ChatCom, Inc., Press Release, Mar. 26, 1996, 2 pages.
- "Astro Sciences Corporation Announces Results for The Third Quarter," Astro Sciences Corporation, Press Release, Feb. 8, 1996, 2 pages.
- "Telecom Australia to Receive Astro Sciences/J&L 486 Services," Astro Sciences Corporation, Press Release, Jan. 4, 1996, 1 page.
- "Astro Sciences Receives Microsoft Certification and Announces New Director," Astro Sciences Corporation, Press Release, Nov. 21, 1995, 2 pages.
- "Astro Sciences Corp. Announces Results for Second Quarter," Astro Sciences Corporation, Press Release, Nov. 17, 1995, 2 pages.
- "Astro Sciences Corp. Signs Agreement With Storage Computer Corp.," Astro Sciences Corporation, Press Release, Nov. 7, 1995, 2 pages.
- "Astro Sciences Corporation Appoints Interim President/CEO Board Expanded by Two Seats," Astro Sciences Corporation, Press Release, Aug. 17, 1995, 1 page.
- "Astro Sciences Corporation Announces Results for the First Quarter of the Fiscal Year," Astro Sciences Corporation, Press Release, Aug. 3, 1995, 1 page.
- "Astro Sciences Corporation Retains Technology Strategies and Alliance Partners," Astro Sciences Corporation, News Release, Jun. 29, 1995, 1 page.
- "Astro Sciences Corporation Receives Patent For Network Security and Management," Astro Sciences Corporation, News Release, Jun. 6, 1995, 2 pages.
- "Astro Sciences Corporation Introduces New Generation of Products at PC Expo Show," Astro Sciences Corporation, Press Release, Jun. 23, 1995, 1 page.
- "Astro Sciences Corporation Announces Results for the Fourth Quarter and the Fiscal Year," Astro Sciences Corporation, News Release, Jun. 26, 1995, 1 page.
- "Astro Sciences Corporation Announces Signing of \$4 Million Credit Facility With Deutsche Financial Services," Astro Sciences Corporation, News Release, May 19, 1995, 1 page.
- "Astro Sciences Corporation to Strengthen Management Team Board," Astro Sciences Corporation, News Release, Apr. 21, 1995, 1 page.
- "J&L Announces their ChatExpress—P75 Applications Server at Networks Expo," J&L Information Systems, Press Release, Feb. 13, 1994, 3 pages.
- "J&L Information Systems Announces two DX4 for their Chat-terBox Family of Remote Access Servers," J&L Information Systems, Press Release, Feb. 13, 1994, 2 pages.
- "J&L Announces the NRS-T10RSTM a Fault Tolerant Applications Server Platform at FOSE," J&L Information Systems, Press Release, Mar. 20, 1994, 2 pages.
- "J&L Announces their ChatAccess™ Family of Remote LAN Node Servers at Network+Intertop Las Vegas," J&L Information Systems, Press Release, Mar. 27, 1994, 2 pages.
- "J&L Announces ChatExpress—P120 Rackmounted Applications Server at PC Expo, New York," J&L Information Systems, Press Release, Jun. 19, 1994, 2 pages.
- "ChatCom Books Additional Orders with Major Facilities—Based Carrier Companies, ChatCom Products Provide Internet Platforms for Carrier's Customers Worldwide," ChatCom, Inc., Press Release, Mar. 12, 1997, 2 pages.
- "ChatCom Announces Comprehensive VAR Program, Commitment to VARs is Key to Corporate Strategy," ChatCom, Inc., Press Release, Jan. 13, 1997, 1 page.



## US RE43,171 E

Page 5

- "ChatCom, Inc. Reports Completion of \$2.5 Million Private Placement," ChatCom, Inc., Press Release, Jan. 9, 1997, 2 pages.
- "ChatCom Announces Mass Storage Subsystem, ChatRAID to Address Application Server Market," ChatCom, Inc., Press Release, Aug. 12, 1996, 1 page.
- "ChatCom, Inc. Announces Commitment to ISO 9001 Quality Certification, ISO 9001 Quality Control Programs are High Priority Company Imperative," ChatCom, Inc., Press Release, Aug. 1, 1996, 1 page.
- "ChatCom Adds New Senior Management Team Members," ChatCom, Inc., Press Release, Jul. 2, 1996, 1 page.
- "ChatCom Announces Mass Storage Subsystem, ChatRAID to Address Application Server Market," ChatCom, Inc., Press Release, Aug. 14, 1996, 2 pages.
- "ChatCom Announces Complete Line of Scaleable Application and Communication Servers," ChatCom, Inc., Press Release, Aug. 30, 1996, 4 pages.
- "ChatCom, Inc. Announces Highly Adaptable Intranet and Web Servers, Servers reduce costs associated with radical change," Press Release, Sep. 3, 1996, 1 page.
- J&L Introduces Twin Pentium for ChatterBox Systems, J&L Information Systems, Press Release, Jan. 29, 1996, 1 page.
- "ChatterBox/SAS™—Scaleable Access Server™," J&L Information Systems, Networks Expo—Boston '96, Dec. 22, 1995, 1 page.
- "J&L Information Systems Announces ChatPower-Plus™ a Revolutionary Redundant Power Supply System," J&L Information Systems, Press Release, Jun. 19, 1995, 2 pages.
- "J&L Announces ChatAccess/PC™, a PCMCIA Based Remote LAN Node Server," J&L Information Systems, Press Release, Jun. 19, 1995, 2 pages.
- "J&L Announces Two Patents," J&L Information Systems, Press Release, Feb. 9, 1995, 1 page.
- "J&L Announces their ChatExpress—P100 Rackmounted Applications Server at Networks Expo. Boston," J&L Information Systems, Press Release, Feb. 13, 1994, 3 pages.
- "J&L Doubles the Rack-Mounted Communications Server Density with ChatVantage/486™," J&L Information Systems, Press Release, Sep. 11, 1995, 2 pages.
- "ChatCom, Inc. Announces Results for the Jun. 30 Quarter," ChatCom, Inc., News Release, Aug. 16, 1996, 2 pages.
- "Introducing the new ChatterBox™ Corporate and Office Series . . . the Power Behind Your Network," ChatCom, Inc., May 31, 1996, 15 pages.
- "ChatterBox Communications and Server Solutions," ChatCom, Inc., Mar. 7, 1996, 12 pages.
- "ChatterBox Communications and Server Solutions Products," ChatCom, Inc., Apr. 24, 1996, 7 pages.
- Lazik, G., "Remote Access—a Historical Perspective," Network News, vol. 3, No. 7, NPA The Network Professional Association, Jul. 1994, 6 pages.
- Lazik, G., "Remote Access—Part II, Cost Analysis," Network News, vol. 3, No. 8, NPA The Network Professional Association, Sep. 1994, 5 pages.
- "Plexnet™ Product Overview," Plexcom, Inc., 1992, 8 pages.
- "Thin Client Servers High-Speed Data Switching Technical Summary," QuantumNet, Inc., Aug. 29, 2010, 28 pages.
- Facsimile from Proccross to Paunovich attaching "QuantumNet Network Computing Systems," Aug. 30, 2010, 8 pages.
- World Wide System Price Guide, Network Engines, Inc., Sep. 26, 1997, 10 pages.
- P6000 System Price Guide, Network Engines, Inc., Feb. 24, 1998, 9 pages.
- "Venture financing is fuel for Powerstation's Growth Plans," Mass High Tech Communications, Inc., Jun. 2, 1997, 1 page.
- Grigonis, R., "Life-Saving Computers: Network Engines," Computer Telephony, Sep. 1997, 1 page.
- Rodgers, A., "NT Clustering Hardware Readied, Vendor Racks up Windows NT Clustering Options at NetWorld+Interop," Internetweek, Oct. 20, 1997, 1 page.
- "Network Engines Awarded Best of Show at Networld + Interop 97, New company debuts product and wins," Network Engines, Inc., Press Release, Oct. 14, 1997, 2 pages.
- Network Engines Website, Network Engines, Inc., [retrieved on Feb. 27, 1998], Retrieved from the Internet: <URL: <http://www.networkengines.com/>>, 12 pages.
- Network Engines, Inc., Company Overview, Aug. 26, 2010, 21 pages.
- Network Engines ClusterDirector Users' Manual, Revision B, Network Engines, Inc., Jun. 1998, 88 pages.
- Network Engines ClusterDirector Users' Manual, Network Engines, Inc., Jan. 1998, 52 pages.
- MP700 User Guide, Issue 0.0.89, Network Engines, Inc., Oct. 16, 1997, 29 pages.
- "ClusterDirector™ Product Description, Fault Tolerance for Industry Standard Processors, Operating Systems, and Applications," Network Engines, Inc., 1998, 4 pages.
- "Network Engines Announces New Clustered Application Servers for Web, Thin-Client and Windows NT Enterprise Environments," Network Engines, Inc., Press Release, Oct. 8, 1997, 3 pages.
- "Network Engines Announces Partnership With Telegration Associates, Inc.," Network Engines, Inc., Press Release, Dec. 10, 1997, 2 pages.
- "Network Engines Debuts ClusterDirector in Internet/Intranet Load Balanced Environment," Network Engines, Inc., Press Release, Jan. 27, 1998, 3 pages.
- Stallings, W., "Computer Organization and Architecture—Designing for Performance," Sixth Edition, Pearson Education, Inc., 2003, pp. 69-89.
- Hill, Goff (editor), "The Cable and Telecommunications Professional's Reference: vol. 1," Third Edition, Focal Press, 2007, pp. 225-229, 7 pages.
- Dell, Inc., White Paper, "PCI Express Technology," Feb. 2004, pp. 1-11.
- Athavale, A., "How to Lower the Cost of PCI Express Adoption by Using FPGAs," EETimes Design [online] Apr. 26, 2006, [retrieved on May 3, 2011], Retrieved from the Internet at <URL: <http://www.eetimes.com/General/DisplayPrintViewContent?contentItemID=4014824>>, 6 pages.
- Thoms, I., "IBM Hit with \$9M Judgment in Server Patent Suit," Law360 [online], [retrieved on May 3, 2011], Retrieved from the Internet at <URL: <http://www.law360.com/articles/229575/print?section=ip>>, 2 pages.
- McKenzie, L., "Fujitsu Reaches Deal in Acqis Blade Server IP Spat," Law360 [online], [retrieved on Jun. 16, 2010], Retrieved from the Internet at <URL: [http://ip.law360.com/print\\_article/175004](http://ip.law360.com/print_article/175004)>, 2 pages.
- PCI Local Bus Specification, Rev. 2.1, The PCI Special Interest Group, Jun. 1, 1995, 298 pages.
- "National Semiconductor Design Guide," LVDS Owner's Manual, Spring 1997, 65 pages.
- Intel Corporation, "PCI Express\* to PCI-X\* Bridge Architecture: Where Interface Standards Meet," 2003, 8 pages.
- Desai, D.M. et al., "BladeCenter system overview," IBM Journal of Research and Development, vol. 49, No. 6, Nov. 2005, pp. 809-821, 13 pages.
- Spring, Tom, "Top of the News—Broadband Users Still Sing the Blues," PC World, Jun. 2011, pp. 42-54, 13 pages.
- San Jose Mercury News, "Business & Stocks—Top Stories from The Mercury News," Jun. 28, 2001, [online], [retrieved on Jun. 30, 2001], Retrieved from the Internet at <URL: <http://www0.mercurycenter.com/premium/business/docs/technews28.htm>>, 5 pages.
- "iMod Pad," Wired Magazine, Mar. 2001, 1 page.
- "Amended Invalidity Chart For Base Reference Network Engines P6000 Server," submitted by the Defendants in connection with Case No. 6:09-cv-148-LED on Jun. 4, 2010, 64 pages.
- Email from Emanuel to Juarez including Invalidity Chart for Base Reference IBM BladeCenter, submitted by the Defendants in connection with Case No. 6:09-cv-148-LED, dated Aug. 20, 2010, 54 pages.
- Letter from Martiniak to Byers regarding Proposed Amendment to the Invalidity Contentions based on products from RLX Systems and a description of RLX products, dated Jul. 15, 2010, 2 pages.
- Defendant's Invalidity Chart for Base Reference RLX System 324, proposed in connection with Case No. 6:09-cv-148-LED on Jul. 15, 2010, 58 pages.

## US RE43,171 E

Page 6

"Disclosure of Asserted Claims and Infringement Contentions," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 5 pages.

"Exhibit 1, Disclosure of Asserted Claims and Infringement Contentions for Defendant Appro International, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 105 pages.

"Exhibit 2, Disclosure of Asserted Claims and Infringement Contentions for Defendant ClearCube Technology, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 163 pages.

"Exhibit 3, Disclosure of Asserted Claims and Infringement Contentions for Defendant Dell Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 184 pages.

"Exhibit 4, Disclosure of Asserted Claims and Infringement Contentions for Defendant Fujitsu America, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 210 pages.

"Exhibit 7, Disclosure of Asserted Claims and Infringement Contentions for Defendant NEC Corp. of America," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 166 pages.

"Exhibit 9, Disclosure of Asserted Claims and Infringement Contentions for Defendant Super Micro Computer, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 220 pages.

"Disclosure of Plaintiff's Reduced List of Asserted Claims," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-00148-LED, served on Jul. 30, 2010, 6 pages.

"Memorandum Opinion and Order Construing Claim Terms and Denying Defendants' Motion for Partial Summary Judgment," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Aug. 2, 2010, 18 pages.

"Jury Verdict Form," Returned by the Jury in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on February 23, 2011, 2 pages.

"Final Judgement," Issued by the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2011, 1 page.

"Complaint for Patent Infringement," *Acqis v. Appro Int'l, Inc. et al.*, Case No. 6:09-cv-00148, filed Apr. 2, 2009, 13 pages.

"First Amended Complaint for Patent Infringement," *Acqis v. Appro Int'l, Inc. et al.*, Case No. 6:09-cv-00148, filed May 18, 2009, 14 pages.

"Defendant Clearcube Technology, Inc.'s Answer, Counterclaims to Acqis LLC's First Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:08-cv-00148, filed Jul. 2, 2009, 28 pages.

"Defendant Nex Computers Technology, Inc.'s Answer to Acqis LLC's First Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:09-cv-00148-LED, filed Jul. 8, 2009, 16 pages.

"Defendant Hitachi Ameirca, Ltd.'s, Answer to Acqis LLC's First Amended Complaint for Patent Infringement, and Affirmative Defenses and Counterclaims," Case No. 6:09-cv-00148-LED, filed Jul. 8, 2009, 22 pages.

"Defendant International Business Machines Corp.'s Answer to Acqis LLC's First Amended Complaint, Affirmative Defenses, and Counterclaims," Case No. 6:09-cv-148-LED, filed Jul. 8, 2009, 22 pages.

"Second Amended Complaint for Patent Infringement," *Acqis v. Appro Int'l, Inc. et al.*, Case No. 6:09-cv-00148, filed Jul. 22, 2009, 49 pages.

"Defendant Appro's Answer, Affirmative Defenses, and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed Aug. 5, 2009, 43 pages.

"Defendant International Business Machines Corp.'s Answer to Acqis LLC's Second Amended Complaint, Affirmative Defenses, and Counterclaims," Case No. 6:09-cv-148-LED, filed Aug. 10, 2009, 28 pages.

"Defendant Super Micro Computer, Inc.'s Answer and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed Aug. 10, 2009, 96 pages.

"Defendant Sun Microsystems, Inc.'s Answer and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148, filed Aug. 10, 2009, 95 pages.

"NEC Corporation of America's Answer, Affirmative Defenses, and Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-00148-LED, filed Aug. 10, 2009, 38 pages.

"Answer to Plaintiff's Second Amended Complaint and Counterclaims of Defendant Fujitsu Computer Systems Corp., n/k/a/ Fujitsu America, Inc. to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-00148-LED, filed Aug. 10, 2009, 34 pages.

"Answer, Affirmative Defenses, and Counterclaims of Defendant Hewlett-Packard Company to Acqis LLC's Second Amended Complaint for Patent Infringement," Case No. 6:09-cv-148-LED, filed Aug. 10, 2009, 40 pages.

"Defendant Clearcube Technology, Inc.'s Answer, Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:08-cv-00148, filed Aug. 10, 2009, 39 pages.

"Dell's Answer and Counterclaims to Acqis LLC's Second Amended Complaint," Case No. 6:09-cv-00148-LED, filed Aug. 10, 2009, 36 pages.

"Defendant Nex Computers Technology, Inc.'s Answer to Acqis LLC's Second Amended Complaint for Patent Infringement, and Jury Demand," Case No. 6:09-cv-00148-LED, filed Aug. 10, 2009, 28 pages.

"Defendant Clearcube Technology, Inc.'s First Amended Answer, Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed Aug. 11, 2009, 39 pages.

"Plaintiff Acqis LLC's Answer to Defendant Appro International, Inc.'s Counterclaims," Case No. 6:09-00148-LED, filed Aug. 28, 2009, 16 pages.

"Defendant Clearcube Technology, Inc.'s Second Amended Answer Counterclaims to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-CV-00148, filed Aug. 31, 2009, 45 pages.

"Plaintiff Acqis LLC's Answer to Defendant International Business Machines Corp.'s Counterclaims," Case No. 6:09-00148-LED, filed Sep. 2, 2009, 11 pages.

"Plaintiff Acqis LLC's Answer to Defendant Super Micro Computer, Inc.'s Counterclaims," Case No. 6:09-00148-LED, filed Sep. 2, 2009, 15 pages.

"Plaintiff Acqis LLC's Answer to Defendant Sun Microsystems, Inc.'s Counterclaims," Case No. 6:09-cv-00148-LED, filed Sep. 2, 2009, 14 pages.

"Plaintiff Acqis LLC's Answer to Defendant Dell Inc.'s Counterclaims," Case No. 6:09-00148-LED, filed Sep. 2, 2009, 16 pages.

"Plaintiff Acqis LLC's Answer to Defendant Fujitsu Computer Systems Corp., N/K/A Fujitsu America, Inc.'s Counterclaims," Case No. 6:09-00148-LED, filed Sep. 16, 2009, 7 pages.

"Plaintiff Acqis LLC's Answer to Defendant Hewlett-Packard Company's Counterclaims," Case No. 6:09-00148-LED, filed Sep. 16, 2009, 14 pages.

"Plaintiff Acqis LLC's Answer to Defendant NEC Corporation of America's Counterclaims," Case No. 6:09-00148-LED, filed Sep. 16, 2009, 8 pages.

"Defendant Clearcube Technology, Inc.'s Third Amended Answer to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed Nov. 11, 2009, 26 pages.

"Defendant Clearcube Technology, Inc.'s Fourth Amended Answer to Acqis LLC's Second Amended Complaint for Patent Infringement and Jury Demand," Case No. 6:09-cv-00148, filed Jan. 8, 2010, 26 pages.

"Dell's First Amended Answer and Counterclaims to Plaintiff's Second Amended Complaint," Case No. 6:09-cv-00148-LED, filed Apr. 22, 2010, 38 pages.

## US RE43,171 E

Page 7

"Plaintiff Acqis LLC's Answer to Defendant Dell Inc.'s First Amended Counterclaims," Case No. 6:09-00148-LED, filed May 10, 2010, 16 pages.

"Affidavit of Timothy P. Cremen in Support of NEC Corporation of America's Opposition to Plaintiff's Motion to Dismiss and Strike," Case No. 6:09-cv-00148-LED, filed Oct. 9, 2009, 4 pages.

"Comparison [by NEC] of Rejected Elements in Office Action and Elements of Exemplary Claims of Acqis's Patents," Case No. 6:09-cv-00148-LED, filed Oct. 9, 2010, 7 pages.

"Defendant NEC Corporation of America's Opposition to Plaintiff's Motion to Dismiss and Motion to Strike," Case No. 6:09-cv-00148-LED, filed Oct. 9, 2010, 36 pages.

"Motion to Dismiss Counterclaim Pursuant to Rule 12(b)(6) and Motion to Strike Affirmative Defense Pursuant to Rule 12(f)," Case 6:09-00148-LED, filed Sep. 16, 2009, 18 pages.

"Transcript of Videotaped Deposition of William Mangione-Smith," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, Sep. 9, 2010, 192 pages.

"Defendant Sun Microsystems, Inc.'s Responses and Objections to Plaintiff Acqis LLC's Second Set of Common Interrogatories," Case No. 6:09-cv-00148-LED, filed May 12, 2010, 9 pages.

"Plaintiff Acqis LLP's Objections and Responses to Defendants' First Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed Aug. 5, 2010, 21 pages.

"Plaintiff Acqis LLP's Objections and Responses to Defendants' Third Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed Aug. 5, 2010, 13 pages.

"Plaintiff Acqis LLP's First Supplemental Objections and Responses to Defendants' Third Set of Interrogatories," Case No. 6:09-cv-00148-LED, filed Aug. 5, 2010, 14 pages.

"Declaration of Jennifer Chen in Support of Defendants' Motion for Leave to Amend Defendants' Invalidity Contentions," Case No. 6:09-cv-00148-LED, Aug. 5, 2010, 3 pages.

Excerpts of Transcript of "Videotaped Deposition of William W.Y. Chu," taken by the Defendants in connection with Case No. 6:09-cv-148-LED in the U.S. District Court for the Eastern District of Texas, Jun. 7, 2010, 20 pages.

"Declaration of Monty McGraw in Support of Defendants' Motion for Leave to Amend Defendants' Invalidity Contentions," Case No. 6:09-cv-00148-LED, Aug. 5, 2010, 3 pages.

"Plaintiff's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed Jun. 1, 2010, 35 pages.

"Declaration of Carolyn V. Juarez in Support of Plaintiff Acqis LLC's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed Jun. 1, 2010, 3 pages.

"Defendant's Brief in Response to Plaintiff's Opening Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed Jun. 15, 2010, 40 pages.

"Proposed Claim Construction Statement," Case No. Case No. 6:09-cv-00148-LED, filed Jun. 15, 2010, 39 pages.

"Claim Chart for International Business Machines Corp.," Case No. 6:09-cv-00148-LED, filed Jun. 15, 2010, 12 pages.

"Acqis LLC's Disclosure of Proposed Terms and Claim Elements For Construction Pursuant to Patent Rule 4-1," Case No. 6:09-cv-00148-LED, filed Mar. 5, 2010, 3 pages.

"Defendant's List of Proposed Terms and Claim Elements for Construction," Case No. 6:09-cv-00148-LED, filed Mar. 5, 2010, 15 pages.

"Defendant's Amended List of Proposed Terms and Claim Elements for Construction," Case No. 6:09-cv-00148-LED, filed Mar. 31, 2010, 11 pages.

"Defendant's Corrected List of Proposed Terms and Claim Elements for Construction," Case No. 6:09-cv-00148-LED, filed Apr. 2, 2010, 9 pages.

"Acqis, LLC's P.R.-4-2 Disclosure of Preliminary Claim Constructions and Extrinsic Evidence," Case No. 6:09-cv-00148-LED, filed Apr. 14, 2010, 10 pages.

"Defendant's P.R.-4-2 Disclosure of Preliminary Claim Constructions and Extrinsic Evidence," Case No. 6:09-cv-00148-LED, filed Apr. 14, 2010, 16 pages.

"Joint Claim Construction Statement," Case No. 6:09-cv-00148-LED, filed Apr. 30, 2010, 46 pages.

"Corrected p. 13 of Plaintiff's Opening Brief Concerning Claim Construction (D.I. 261)," Case No. 6:09-cv-00148-LED, filed Jun. 2, 2010, 2 pages.

"Plaintiffs Reply Brief Regarding Claim Construction," Case No. 6:09-cv-00148-LED, filed Jun. 28, 2010, 14 pages.

Final Office Action for U.S. Appl. No. 12/561,138, mailed Mar. 17, 2011, 5 pages.

Agerwala, T. et al., "SP2 System Architecture", IBM Systems Journal, vol. 34, No. 2 (1995).

Bernal, Carlos, product brochure entitled: "PowerSMP Series 4000", (Mar. 1998) <<<http://www.winnetmag.com/Windows/Article/ArticleID/3095/3095.html>>>, downloaded from web on Jun. 22, 2004, 2 pgs.

Cragle, Jonathan, "Density System 1100", (May 1999) <<<http://www.winnetmag.com/Windows/Article/ArticleID/5199/5199.html>>>, downloaded from web on Jun. 21, 2004, 3 pgs.

Feldman, Jonathan, "Rack Steady: The Four Rack-Mounted Servers That Rocked Our Network", <<<http://www.networkcomputing.com/shared/printArticle.jhtml?article=/910/910r3side1.htm...>>> Jun. 23, 2004, 3 pgs.

Fetters, Dave, "Cubix High-Density Server Leads the Way With Standout Management Software", (Feb. 8, 1999) <<<http://www.nwc.com/shared/printArticle.jhtml?article=/1003/1003r3full.html&pub=nwc>>>, downloaded from web on Jun. 23, 2004, 5 pgs.

Gardner, Michael and Null, Christopher, "A Server Condominium", <<<http://www.lantimes.com/testing/98jun/806a042a.html>>>, Jun. 23, 2004, 3 pgs.

Harrison, Dave, "VME in the Military: The M1A2 Main Battle Tank Upgrade Relies on COTS VME" <<<http://www.dy4.com>>>, (Feb. 9, 1998), pp. 1-34.

Williams, Dennis, "Consolidated Servers", (Feb. 17, 1997) <<<http://www.lantimes.com/testing/97compare/peconsol.html>>> downloaded from web on Jun. 23, 2004, 2 pgs.

Williams, Dennis, "Executive Summary: Consolidate Now", (Feb. 17, 1997) <<<http://www.lantimes.com/testing/97feb/702b064a.html>>> downloaded from web on Jun. 23, 2004, 2 pgs.

Williams, Dennis, "Top "Scores for Useability and Openness", (Feb. 17, 1997) <<<http://www.lantimes.com/testing/97feb/702b064a.html>>> downloaded from web on Jun. 23, 2004, 2 pgs.

Williams, Dennis, "ChatCom Inc. Chatterbox", (Feb. 17, 1997) <<<http://www.lantimes.com/testing/97feb/702b066a.html>>> downloaded from web on Jun. 23, 2004, 3 pgs.

Williams, Dennis, "Eversys Corp. System 8000", (Feb. 17, 1997) <<<http://www.lantimes.com/testing/97feb/702b070b.html>>> downloaded from web on Jun. 22, 2004, 4 pgs.

Williams, Dennis, "Cubix Corp. ERS/FT II", (Feb. 17, 1997) <<<http://www.lantimes.com/testing/97feb/702b068b.html>>> downloaded from web on Jun. 23, 2004, 4 pgs.

Crystal Group, "Rackmount Computers", (© 2000-2004) <<<http://www.crystalpc.com/products/roservers.asp>>>, downloaded from web on Jun. 17, 2004, 8 pgs.

Crystal Group, "QuickConnect® Cable Management", (© 2000-2004) <<<http://www.crystalpc.com/products/quickconnect.asp>>> downloaded from web on Jun. 17, 2004, 4 pgs.

Cubix Product Brochure entitled, "Density System", (© 2000) <<<http://64.173.211.7/support/techinfo/system/density/density10.htm>>> downloaded from web on Jun. 22, 2004, 3 pgs.

Cubix Product Brochure entitled, "Density System, Technical Specifications", (©2000) <<<http://64.173.211.7/support/techinfo/system/density/info/spec.htm>>> downloaded from web on Jun. 22, 2004, 2 pgs.

Cubix Product Manual entitled, "Density System", Chapter 1—Introduction, (© 2000) <<<http://64.173.211.7/support/techinfo/manuals/density/Chap-1.htm>>> downloaded from web on Jun. 22, 2004, 5 pgs.

Cubix, "Click on the front panel that matches your system", (© 2000) <<<http://64.173.211.7/support/techinfo/system/density/densiry.htm>>>, downloaded from web on Jun. 22, 2004, 1 pg.

Cubix Product Manual entitled, "Density System", Chapter 2—Installation, (© 2000) <<<http://64.173.211.7/support/techinfo/manuals/density/Chap-2.htm>>> downloaded from web on Jun. 22, 2004, 9 pgs.



## US RE43,171 E

Page 8

Cubix Product Manual entitled, "Density System", Chapter 3—Operation, (© 2000) <<<http://64.173.211.7/support/techinfo/manuals/density/Chap-3.htm>>> downloaded from web on Jun. 22, 2004, 4 pgs.

Cubix Product Manual entitled, "Density System", Chapter 4—Maintenance and Repair, (© 2000) <<<http://64.173.211.7/support/techinfo/manuals/density/Chap-4.htm>>> downloaded from web on Jun. 22, 2004, 5 pgs.

Cubix, "What are Groups?", (© 2000) <<<http://64.173.211.7/support/techinfo/system/density/info/groups.htm>>>, downloaded from web on Jun. 22, 2004, 3 pgs.

Cubix, "SP 5200XS Series Plug-in Computers", (© 2000) <<<http://64.173.211.7/support/techinfo/bc/sp5200xs/intro.htm>>>, downloaded from web on Jun. 22, 2004, 2 pgs.

Cubix, "SP 5200XS Series Technical Specifications", (© 2000) <<<http://64.173.211.7/support/techinfo/bc/sp5200xs/spec.htm>>>, downloaded from web on Jun. 22, 2004, 2 pgs.

Cubix, "SP 5200 Series" Chapter 1—Introduction, (© 2000) <<<http://64.173.211.7/support/techinfo/manuals/s5200/chap-1.htm>>>, downloaded from web on Jun. 22, 2004, 3 pgs.

Cubix, "SP 5200 Series" Chapter 2—Switches & Jumpers, (© 2000) <<<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-2.htm>>>, downloaded from web on Jun. 22, 2004, 3 pgs.

Cubix, "SP 5200 Series" Chapter 3—Installation, (© 2000) <<<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-3.htm>>>, downloaded from web on Jun. 22, 2004, 4 pgs.

Cubix, "SP 5200 Series" Chapter 4—Technical Reference, (© 2000) <<<http://64.173.211.7/support/techinfo/manuals/sp5200/chap-4.htm>>>, downloaded from web on Jun. 22, 2004, 3 pgs.

Cubix, "DP 6200 'D' Series Plug-in Computers" <<<http://64.173.211.7/support/techinfo/bc/dp6200d/intro.htm>>>, downloaded from web on Jun. 22, 2004, 3 pgs.

Cubix, "Installing DP or SP Series Boards" (© 2000) <<<http://64.173.211.7/support/techinfo/bc/dp6200d/intro.htm>>>, downloaded from web on Jun. 22, 2004, 2 pgs.

Cubix, "Powering On/Off or Resetting Plug-in Computers in an Density System", (© 2000) <<<http://64.173.211.7/support/techinfo/system/density/info/power.htm>>>, downloaded from web on Jun. 22, 2004, 2 pgs.

Cubix, "Multiplexing Video, Keyboard & Mouse with Multiple Density Systems", (© 2000) <<<http://64.173.211.7/support/techinfo/system/density/info/vkm-mux.htm>>>, downloaded from web on Jun. 22, 2004, 2 pgs.

eBay Advertisement for "Total IT Group Network Engines", <<<http://cgi.ebay.com/we/eBayISAPI.dll?ViewItem&item=5706388046&sspageName=STRK%3AMDBI%3AMEBI3AIT&rd=1>>>, downloaded from web on Jun. 25, 2004, 1 pg.

"Features Chart", (Feb. 1, 1997) <<<http://lantimes.com/testing/97feb/702b072a.html>>>, downloaded from web on Jun. 23, 2004, 3 pgs.

Internet Telephony Roundup, "Industrial Computers" <<<http://www.tmcnet.com/articles/itmag/0499/0499roundup.htm>>>, downloaded from web on Jun. 23, 2004, pp. 1-5.

Press Release: "Crystal Group Products Offer Industrial PCs with Built-in Flexibility", Hiawatha, Iowa, (Mar. 1, 1997) <<<http://www.crystalpc.com/news/pressreleases/prodpr.asp>>>, downloaded from web on May 14, 2004, 2 pgs.

Press Release: "Enhanced COTS SBC from DY 4 Systems features 166MHz Pentium™ Processor" Kanata, Ontario, Canada, (Apr. 1998) <<<http://www.realtime-info.be/VPR/layout/display/pr.asp?PRID=363>>>, 2 pgs.

DY 4 Systems, Inc., SVM/DM-192 Pentium® II Single Board Computer (Jun. 1999) pp. 1-9.

Bomara Associates, "System 8000", <<<http://www.bomara.com/Eversys/briefDefault.htm>>>, downloaded from web on Jun. 22, 2004, 4 pgs.

Cubix, "ERS/FT II System", (© 2000) <<<http://64.173.211.7/support/techinfo/system/ersft2/ersft2.htm>>>, downloaded from web on Jun. 22, 2004, 4 pgs.

Cubix, "ERS II and ERS/ FT II", Chap. 3, System Components, <<<http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c3.htm>>>, downloaded from web on Jun. 22, 2004, 21 pgs.

Product Manual entitled: "ERS II and ERS/FT II", Chap. 6, Component Installation, <<<http://64.173.211.7/support/techinfo/manuals/ers2/ers2-c6.htm>>>, downloaded from web on Jun. 22, 2004, 18 pgs.

Windows Magazine, "Cubix PowerSMP Series 4000", Nov. 1997, <<http://www.techweb.com/winmag/library/1997/1101/ntent008.htm>>> downloaded from the web on Jun. 22, 2004, p. NT07.

CETIA Brochure "CETIA Powerengine CVME 603e" pp. 1-6 downloaded from the internet @ [http://www.cetia.com/Products\\_Addons/wp-47-01.pdf](http://www.cetia.com/Products_Addons/wp-47-01.pdf) on Feb. 15, 2006.

MPL Brochure, "The First Rugged AI in One Industrial 486FDX-133 Mhz PC", (1998), pp. 53.

MPL Brochure "IPM 486 Brochure/IPM5 User Manual", pp. 1-9, downloaded from the internet @ <http://www.mplch/DOCS/u48600xd.pdf> on Feb. 15, 2006.

Snyder, Joel, "Better Management Through Consolidation," pp. 1-6 <http://www.opus1.com/www/jms/nw-con-0818rev.html>. (Aug. 18, 1997).

Eversys Corporation, "Eversys System 8000 Consolidated Network Server Market and Product Overview," Slide presentation, downloaded from <<http://eversys.com>>, product to be released Mar. 1, 1997, 20 pages (no date on document).

"SQL Server and NT Cluster Manager Availability Demo," Microsoft Server Programmer Developers Conference, Nov. 1996, 15 pages.

HP: HDMP-1636, Gigabit Ethernet Transceiver Chip, Preliminary Technical Data (May 1997) (No. 123.pdf).

ACCTON, Gigabit Ethernet PCI Adapter (1999) (2 pp) (No. 122.pdf).

Intel, 82559 Fast Ethernet Multifunction PCI/Cardbus Controller (Jan. 1999) (56 pp.) (No. 128.pdf).

Intel, 21143 PCI/CardBus 10/100Mb/s Ethernet LAN Controller, Product Datasheet (Oct. 1998) (8 pp.) (No. 127.pdf).

KTI Networks, Installation Guide 10/100 Dual-speed Fast Ethernet PCI Adapters (1999) (24 pp.) (No. 126.pdf).

Micronet SP2500R Series Etherfast 10/100 MBPS Adapter, User's Guide (1999) (10 pp.) (No. 136.pdf).

PCI Local Bus Specification (Rev. 2.2, Dec. 1998) (322 pp.) (No. 135.pdf).

EIA-422A—Standard (Superseded), Electrical Characteristics of Balanced Voltage Digital Interface Circuits (Dec. 1978) (20 pp) (No. 118a.pdf).

TIA/EIA (644) Standard Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits (Mar. 1996) (42 pp) (No. 118c.pdf).

Huq et al. "An Overview of LVDS Technology" National Semiconductor Corp. (Jul. 1998) (6 pp.) (No. 118d.pdf).

Ziatech Corporation—Ketris9000 Product Manual (2000) (159 pp.) (No. 18.pdf).

Ziatech Corp. ZT 8907 Product Description (1998) (4 pp) (No. 19b.pdf).

Ziatech Corp. ZT 8908 Product Description (1998)+A249 (6 pp) (No. 19c.pdf).

Ziatech Corp. System Designer's Guide: Hot Swap Capability on STD 32 Computers (Jan. 1996) (6 pp) (No. 19e.pdf).

Ziatech Corp. Press Release (Feb. 1996) (2 pp.) (No. 19i.pdf).

Ziatech Corp. Industrial BIOS for CompactPCI and STD 32 Systems Software Manual (Jul. 1998) (134 pp) No. 19h.pdf).

Ziatech Corp. System Designers Guide: Expanding STD Bus Performance Through Multiprocessing. (Apr. 1996) (6 pp.) (No. 19d.pdf).

Network Engines: P6000EXP Fault—Tolerant Load—Balanced Cluster Server (NEI00095) (1997) (4 pp.) (No. 22a.pdf).

Whitecross Data Exploration Configuration and Maintenance Manual. Draft. (Jul. 2000) (699 pp.) (No. 26e.pdf).

Whitecross WX-DES Hardware Maintenance (2000) (284 pp) (No. 26g.pdf).

Whitecross WX-DES Technical Overview (2000) (211 pp) (No. 26h.pdf).

8260 ATM Product Architecture, IBM International Technical Support Organization, Raleigh Center, Sep. 1997, First Edition, International Business Machines Corporation, 220 pages.

8265 Nways ATM Switch, Product Description, Sep. 1998, Fifth Edition, International Business Machines Corporation, 141 pages.

## US RE43,171 E

Page 9

- Origin2000 Rackmount Owner's Guide, Document No. 007-3456-003, 1997, Silicon Graphics, Inc., 146 pages.
- QuantumNet, Inc., QuantumNet Product Overview [online], 1996 [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19971011194003/www.quantumnet.com/product.htm>>, 1 page.
- QuantumNet, Inc., QuantumNet: The Next Generation Computing and Networking Environment [online], 1996 [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19971011194123/www.quantumnet.com/qnetovw.htm>>, 7 pages.
- QuantumNet, Inc., QuantumNet 6500 Processor Modules [online], 1996 [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19971011194317/www.quantumnet.com/ds6500.htm>>, 4 pages.
- QuantumNet, Inc., QuantumServer Chassis [online], 1996 [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19971011194309/www.quantumnet.com/dsq6000.htm>> 3 pages.
- Cubix Corporation, White Paper: Benefits of High-Density Servers [online], 1997 [retrieved on Jul. 31, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970716204215/www.cubix.com/corporate/whitepaper/densit.htm>>, 6 pages.
- Cubix Corporation, Datasheet: Single—Board Computers with Pentium Processors [online], 1997 [retrieved on Jul. 31, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970716204717/www.cubix.com/corporate/data/bcp5ft.htm>>, 5 pages.
- Cubix Corporation, Datasheet: ERS/FT II Server Chassis [online], 1997 [retrieved on Jul. 31, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970716204623/www.cubix.com/corporate/data/ersft2.htm>>, 3 pages.
- Cubix Corporation, Cubix ERS/FT II Systems [online], 1997 [retrieved on Jul. 31, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19980124213320/www.cubix.com/support/steps/ers-ft2/intro.htm>>, 5 pages.
- Cubix Corporation, Cubix Product Catalog, Summer 1995, 56 pages.
- Cubix Corporation, BC Series, Processor Boards Installation Guide, DOC 800A, Aug. 1994, 149 pages.
- Cubix Corporation, ERS/FT II—Enhanced Resource Subsystem/Fault Tolerant II, Nov. 1994, 4 pages.
- Cubix Corporation, Density Series Plug-In Servers, Plug-In Computers for Managed Server Farms, Sep. 15, 1998, 2 pages.
- Cubix Corporation, Cubix Pentium II Plug-In Computers for Density Series Systems, Sep. 15, 1998, 1 page.
- Cubix Corporation, Density Series Multi-Server Systems, Sep. 10, 1999, 4 pages.
- Compaq Computer Corporation, White Paper, “Order and Configuration Guide for Compaq ProLiant Cluster Series F Model 100,” Sep. 1998, pp. 1-8.
- Compaq Computer Corporation, QuickSpecs, Compaq ProLiant Cluster Series F Model 100, (undated), pp. 8-36 to 8-37.
- Compaq Computer Corporation, Compaq Performance Brief, ProLiant 1600 ServerBench Performance Summary, Aug. 1998, pp. 1-7.
- Compaq Computer Corporation, Compaq ActiveAnswers Installation Guide, Installation and Configuration Guide for Linux and Apache Web Server on Compaq Prosignia and ProLiant Servers, May 1999, pp. 1-40.
- Compaq Computer Corporation, Compaq White Paper, “Microsoft Internet Information Server 4.0 on the Compaq ProLiant 6500,” Aug. 1998, pp. 1-14.
- Compaq Computer Corporation, Compaq White Paper, “Accelerating Financial Spreadsheet Simulations with Workstation Clusters,” Oct. 1998, pp. 1-14.
- Compaq Computer Corporation, ProLiant 6500-PDC/O1000 C/S with 4 ProLiant 1850R, TPC-C Rev. 3.4, Report Date: Dec. 22, 1998, pp. 1-3.
- Black Box Corporation, Black Box Network Services, Black Box ServSwitch Duo, Jul. 1998, 52 pages.
- Compaq Computer Corporation, Compaq White Paper, “ServerNet—A High Bandwidth, Low Latency Cluster Interconnection,” Sep. 1998, pp. 1-9.
- JL ChatCom, Inc.—Web Site, JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], 1996 [retrieved on Dec. 2, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970104221841/www.jlchatcom.com/>>, 1 page.
- JL ChatCom, Inc.—Scaleable Application and Communication Servers, “ChatCom, Inc. Announces Complete Line of Scaleable Application and Communication Servers,” Aug. 30, 1996 [retrieved on Dec. 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970104221932/www.jlchatcom.com/cpofrel.htm>>, 4 pages.
- JL ChatCom, Inc.—Highly Adaptable Intranet and Web Servers, “ChatCom, Inc. Announces Highly Adaptable Intranet and Web Servers,” Sep. 3, 1996 [retrieved on Dec. 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970104221941/www.jlchatcom.com/chat4int.htm>>, 2 pages.
- JL ChatCom, Inc., “ChatPower Plus,” 1996 [retrieved on Dec. 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970104222122/www.jlchatcom.com/chatplus.htm>>, 3 pages.
- JL ChatCom, Inc., “ChatterBox ChatPower Plus,” (undated) [retrieved on Dec. 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970104222556/www.jlchatcom.com/cpl.gif>>, 1 page.
- JL ChatCom, Inc., “ChatExpress PB5 Series P166 Pentium PCI/ISA CPU Card,” 1996 [retrieved on Dec. 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970104222157/www.jlchatcom.com/chat599.htm>>, 2 pages.
- JL ChatCom, Inc., “ChatExpress—2 Slot,” [retrieved on Dec. 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970104222644/www.jlchatcom.com/exp211.gif>>, 1 page.
- Intel Corporation, Intel 82559 Fast Ethernet Multifunction PCI/Cardbus Controller, Networking Silicon, Preview Datasheet, Jan. 1999, 56 pages.
- Ziatech Corporation, STD 32 zVID2 Local Bus Super VGA/FPD Adapter, Apr. 1996, 2 pages.
- Wolfpack or Microsoft Cluster Services on Star System, (undated), 3 pages.
- Network Engines, Inc., Network Engines ClusterDirector User's Manual, Jun. 1998, 32 pages.
- Eversys Corporation, System 8000 Consolidated Network Server Product Brief, (undated), 2 pages.
- Eversys Corporation, System 8000 Consolidated Server, (undated), [retrieved on Nov. 9, 2009], Retrieved from C: drive <path: file://C:\Documents and Settings\Daniel\M Documents\Eversys\Eversys Web Site Master...>, 6 pages.
- Eversys Corporation, System 8000 Consolidated Server Presentation, (undated), 23 pages.
- Eversys Corporation, System 8000 Consolidated Network Server, Pentium II Processor Module User's Guide for Module version P2D-BXT, Jan. 1998, 49 pages.
- Eversys Corporation, Eversys System 8000 Peripheral Sharing Switch (PSS) User's Guide, 1st Edition—Jun. 1997, 2nd Edition—Jan. 1998, 17 pages.
- Eversys Corporation, WebView 8000 version 1.1 User's Guide, Web-Based Management Software for the Eversys System 8000 Consolidated Server, Revision A—Nov. 1998, Revision B—Dec. 1998, 56 pages.
- Eversys Corporation, S8000 Single Module Body Assembly, Oct. 9, 1998, 9 pages.
- Eversys CAPserver Product Brief [online], (undated), [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19961104093115/www.eversys.com/CAPbrief.htm>>, 10 pages.

## US RE43,171 E

Page 10

- Eversys CAPcard 9500/sa Product Brief [online], (undated), [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: [http://web.archive.org/web/19961104093144/www.eversys.com/cc95sa\\_Brief.htm](http://web.archive.org/web/19961104093144/www.eversys.com/cc95sa_Brief.htm)>, 3 pages.
- Evergreen Systems, Inc., "CAPserver, The Communication/Application server for local area networks," Product Guide, (undated), 18 pages.
- Phillips, J., "9800 Disk Card Design Specification," May 26, 1998, White Cross Systems Limited, pp. 1-44.
- Phillips, J., "9800 Disk Card Layout Specification," Apr. 6, 1998, White Cross Systems Limited, pp. 1-22.
- Feakes, L., "Disk Connector Card Functional Requirement Specification," Jan. 14, 1998, White Cross Systems Limited, pp. 1-4.
- Feakes, L., "Disk Connector Card Layout Specification," Jan. 14, 1998, White Cross Systems Limited, pp. 1-6.
- Burrow, M., WhiteCross Data Exploration, "A Technical Overview of the WXDES/9800," Mar. 2, 1999, Revision 2.00, White Cross Systems Limited, pp. 1-90.
- Burrow, M., WhiteCross Data Exploration, "A Technical Overview of the WXDES/9800," Apr. 21, 1999, White Cross Systems Limited, 222 pages.
- Khan, M. F., "Ethernet Switch Card Design Specification," Mar. 8, 2001, White Cross Systems Limited, pp. 1-32.
- Khan, M. F., "Ethernet Switch Card Layout Specifications," Mar. 8, 2001, pp. 1-31.
- Smith, B., Processor Backplane Functional Requirement Specification, Jul. 31, 1997, White Cross Systems Limited, pp. 1-11.
- Smith, B., "Processor Backplane Design Specification," Feb. 3, 1998, White Cross Systems Limited, pp. 1-16.
- Smith, B., "Processor Backplane Layout Specification," Nov. 12, 1997, White Cross Systems Limited, pp. 1-7.
- Phillips, J., "9800 Processor Card Design Specification," Feb. 25, 1998, White Cross Systems Limited, pp. 1-41.
- Phillips, J., "9800 Processor Card Layout Specification," Sep. 29, 1997, White Cross Systems Limited, pp. 1-13.
- Miastkowski, S. (Editor), "A Whale of a System," Byte, Aug. 1991, 4 pages, vol. 16, No. 8.
- Advanced Micro Devices, Inc., "AMD-K6-III Processor Data Sheet," 21918B/0, Oct. 1999, 326 pages.
- Black Box Corporation, "Black Box Serve Switch Duo," Black Box Network Services Manual, Jul. 1998, 52 pages.
- Cisco Systems, Inc., "Cisco AS5800 Universal Access Server Dial Shelf Controller Card Installation and Replacement," Doc. No. 78-4653-02, 1997, 28 pages.
- Digital Equipment Corporation, "Digital AlphaServer 4000 and 4100 systems," [Brochure], 1998, 4 pages.
- Eversys, "CAPserver Product Brief" [online], [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19961104093115/www.eversys.com/CAPbrief.htm>>, 10 pages.
- Eversys, "CAPcard 9500/sa Product Brief," [online], [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: [http://web.archive.org/web/19961104093144/www.eversys.com/cc95sa\\_Brief.htm](http://web.archive.org/web/19961104093144/www.eversys.com/cc95sa_Brief.htm)>, 3 pages.
- Evergreen Systems, Inc., "CAPserver, The Communication/Application server for local area networks," Product Guide, (undated), 18 pages.
- Grow, R. et al., "Gigabit Media Independent Interface Proposal," Nov. 11, 1996, IEEE 802.3Z, Vancouver, 22 pages.
- Intel, "Pentium® II Processor at 350 MHz, 400 MHz, and 450 MHz, Datasheet," Order No. 243657-003, Aug. 1998, 83 pages.
- Ellis, S., "IRIS FailSafe™ Administrator's Guide," Document No. 007-3109-003, Apr. 6, 1997, 212 pages.
- NEC, "Server HX4500 User's Guide," PN: 456-00005-000, Dec. 1998, 160 pages.
- Novell, Inc., "Novell's NetWare 4.1 Momentum Continues—NetWare 4 Now World's Best-Selling Network Operating System," [online], Mar. 21, 1996, [retrieved on Nov. 16, 2009]. Retrieved from the Internet: <URL: <http://www.novell.com/news/press/archive/1996/03/pr96056.html>>, 2 pages.
- Chapter 7: Maintaining the NetWare Server, "Supervising the Network," (undated), pp. 514-517.
- Chapter 7: Designing a Data Protection Plan, (undated), pp. 170-171.
- Concepts, Disk Driver and Disk Duplexing, (undated), pp. 82-83.
- Network Engines, "P6000EXP Fault-tolerant Load-balanced Clustered Server," 1997, 3 pages.
- Sun Microsystems Computer Company, "Sun™ Enterprise™ 250 Server Owner's Guide," Jun. 1998, Part No. 805-5160-10, Revision A, 324 pages.
- Sun Microsystems, Inc., "UltraSPARC™—II CPU Module, Datasheet 400 MHz CPU, 2.0 MP E-Cache," Jul. 1999, 28 pages.
- Sun Microsystems, Inc., White Paper, "Netra™ ft 1800," Apr. 1999, Revision 09, 50 pages.
- Compaq Computer Corporation, et al., "Universal Serial Bus Specification," Sep. 23, 1998, Revision 1.1, 327 pages.
- Compaq Computer Corporation, et al., "Universal Serial Bus Specification," Apr. 27, 2000, Revision 2.0, 650 pages.
- Silicon Graphics International, "Additional Information for: IRIS FailSafe Administrator's Guide (IRIX 6.4)," [online], Document No. 007-3109-003, Published Apr. 6, 1997, [retrieved on Nov. 5, 2009], Retrieved from the Internet: <URL: <http://techpubs.sgi.com/library/tpl/cgi-bin/summary.cgi?coll=0640&db=bks&docnumber=...>>, 2 pages.
- Origin and Onyx Theory of Operations Manual, Document No. 007-3439-002, 1997, Silicon Graphics, Inc., 124 pages.
- QuantumNet, Inc., QuantumNet 6000 Sharing Modules [online], 1996 [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19971011194326/www.quantumnet.com/dsq60xx.htm>>, 3 pages.
- JL ChatCom, Inc., "ChatTwin," [retrieved on Dec. 2, 2009], JL ChatCom, Inc., ChatterBox Communications and Server Solutions [online], Retrieved from the Internet: <URL: <http://web.archive.org/web/19970104222644/www.jlchatcom.com/chattwin.htm>>, 2 pages.
- Eversys, "Welcome to EverSys" [online], [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19961.104092834/www.eversys.com/index2.htm>>, 1 page.
- Eversys, "Products" [online], [retrieved on Nov. 16, 2009], Retrieved from the Internet: <URL: <http://web.archive.org/web/19961104093103/www.eversys.com/prodinfo.htm>>, 2 pages.
- "Microsoft Press Computer Dictionary, Third Edition," Microsoft Press, 1997, pp. 199 and 332, Kim Fryer ed.
- Excerpt from "Microsoft Computer Dictionary, 5th Edition," Microsoft Press, 2002, pp. 96 and 547.
- Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pp. 78, 79 and 128.
- Anderson, C.R. et al., "IEEE 1355 HS-Links: Present Status and Future Prospects," [online], 1998, [retrieved on Aug. 11, 2010], Retrieved from the Internet: <URL: <http://www94.web.cern.ch/HIS/dshs/publications/wotug21/hslink/pdf/hslinkpaper.pdf>>, 14 pages.
- Mamakos, L. et al., "Request for Comments 2516—A method for Transmitting PPP Over Ethernet (PPPoE)," [online], 1999, [retrieved on Aug. 18, 2010], Retrieved from the Internet: <URL: <http://tools.ietf.org/html/rfc2516>>, 35 pages.
- Haas, S., "The IEEE 1355 Standard: Developments, Performance and Application in High Energy Physics," Thesis for degree of Doctor of Philosophy, University of Liverpool, Dec. 1998, 138 pages.
- "IEEE Std 1355-1995 Standard for Heterogeneous InterConnect (HIC)," Open Micro-processor systems Initiative (OMI), [online], Oct. 30, 1998, [retrieved on Aug. 6, 2010], Retrieved from the Internet: <URL: <http://grouper.ieee.org/groups/1355/index.html>>, 6 pages.
- Galles, M., "Spider: A Hide-Speed Network Interconnect," IEEE Micro, 1997, pp. 34-39. (6 pages).
- Excerpt from "Microsoft Computer Dictionary, 4th Edition," Microsoft Press, 1999, pp. 184-185, 241, 432 (7 pages).
- Excerpt from "Microsoft Computer Dictionary, 4th Edition," Microsoft Press, 1999, pp. 40, 241, 432 (6 pages).
- Excerpt from IEEE 100: The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000), pp. 181, 304 and 771.
- "Family of VME Technology Specifications," [online], date unknown, [retrieved on Dec. 29, 2010], Retrieved from the Internet: <URL: <http://www.vita.com/specifications.html>>, 1 page.
- Cubix Customer Service Support System, "Click on the Front Panel That Matches Your System," © 2000, Cubix [online], [retrieved on



**US RE43,171 E**

Page 11

Jun. 22, 2004]. Retrieved from the Internet at <URL: <http://64.173.211.7/support/techinfo/density/density.htm>>, 1 page.

International Search Report for International Patent Application No. PCT/US99/09369, report mailed Nov. 16, 1999, 7 pages.

International Preliminary Examination Report for International Patent Application No. PCT/US99/09369, report completed Jul. 5, 2000, 4 pages.

IBM Corporation, "Grounding Spring for Peripheral Device and Bezel Bracket," IBM Technical Disclosure Bulletin, Nov. 1, 1993, vol. 36, No. 11, 2 pages.

Digital Semiconductor Product Brief, "21152 PCI-to-PCI Bridge," Feb. 1996, 6 pages.

Intel Corporation Architectural Overview, "Intel 430TX PCISSET: 82439TX System Controller (MTXC)," Feb. 1997, 4 pages.

Intel Corporation Architectural Overview, "Intel 82371AB PCI-to-ISA/IDE XCEL-ERATOR (PIIX4)," Apr. 1997, 3 pages.

Intel Corporation Advance Information, "Intel 440LX AGPSET: 82443LX PCI A.G.P. Controller (PAC)," Aug. 1997, 4 pages.

National Semiconductor, DS90CR215/DS90CR216 +3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link-66 MHz, Jul. 1997, 2 pages.

National Semiconductor Product Folder, "DS90CR215 Plus-3.3V Rising Edge Data Strobe LVDS 21-Bit Channel and Link—66 MHz," National Semiconductor Corporation [online], [retrieved on Oct. 30, 1997]. Retrieved from the Internet at <URL: <http://www.national.com/search/search.cgi/design?keywords=DS90CR215>>, 2 pages.

Video Electronics Standards Association (VESA), Plug and Display (P&D) Standard, P&D and Digital Transition Minimized Differential Signaling (TMDS) Video Transmission Overview, 1997, Version 1, Revision 0, pp. 13 & 31-34.

Office Action for U.S. Patent No. 6,718,415, mailed Oct. 10, 2002, 7 pages.

Response for U.S. Patent No. 6,718,415, filed Nov. 7, 2002, 9 pages.

Office Action for U.S. Patent No. 6,718,415, mailed Jan. 29, 2003, 7 pages.

Response for U.S. Patent No. 6,718,415, filed Mar. 6, 2003, 8 pages.

Office Action for U.S. Patent No. 6,718,415, mailed Jun. 4, 2003, 8 pages.

Response for U.S. Patent No. 6,718,415, filed Sep. 4, 2003, 10 pages.

Amendment Submitted With RCE for U.S. Patent No. 7,099,981, filed Mar. 1, 2006, 23 pages.

Office Action for U.S. Patent No. 7,363,415, mailed on Apr. 12, 2007, 23 pages.

Response for U.S. Patent No. 7,363,415, filed on Apr. 24, 2007, 25 pages.

Office Action for U.S. Patent No. 7,328,297, mailed Feb. 8, 2007, 5 pages.

Response for U.S. Patent No. 7,328,297, filed Apr. 19, 2007, 32 pages.

Office Action for U.S. Patent No. 7,328,297, mailed Jul. 12, 2007, 13 pages.

Response for U.S. Patent No. 7,328,297, filed Jul. 23, 2007, 20 pages.

Office Action for U.S. Patent No. 7,363,416, mailed Apr. 12, 2007, 23 pages.

Response for U.S. Patent No. 7,363,416, filed Apr. 24, 2007, 23 pages.

Office Action for U.S. Patent No. 7,376,779, mailed Sep. 28, 2007, 24 pages.

Response for U.S. Patent No. 7,376,779, filed Oct. 16, 2007, 23 pages.

Office Action for U.S. Patent No. 7,676,624, mailed Dec. 1, 2008, 8 pages.

Response for U.S. Patent No. 7,676,624, filed Jan. 13, 2009, 14 pages.

Supplemental Response for U.S. Patent No. 7,676,624, filed on Feb. 6, 2009, 13 pages.

Office Action for U.S. Patent No. 7,818,487, mailed Sep. 29, 2009, 10 pages.

Response for U.S. Patent No. 7,818,487, filed Nov. 6, 2009, 3 pages.

Amendment for U.S. Patent No. 7,818,487, filed May 11, 2010, 15 pages.

Amendment Submitted After Notice of Allowance for U.S. Patent No. 7,818,487, filed Aug. 17, 2010, 14 pages.

Office Action for U.S. Publication No. 2010/0174844, mailed Oct. 28, 2010, 11 pages.

Office Action for U.S. Patent No. 6,216,185, mailed Apr. 12, 2000, 9 pages.

Response for U.S. Patent No. 6,216,185, filed Aug. 3, 2000, 15 pages.

Office Action for U.S. Patent No. 6,216,185, mailed Aug. 25, 2000, 9 pages.

Response for U.S. Patent No. 6,216,185, filed Oct. 24, 2000, 10 pages.

Office Action for U.S. Patent No. 6,345,330, mailed Jun. 15, 2000, 7 pages.

Amendment for U.S. Patent No. 6,345,330, filed Sep. 12, 2000, 5 pages.

Restriction Requirement for U.S. Patent No. 6,345,330, mailed Dec. 19, 2000, 5 pages.

Amendment filed with Continued Prosecution Application for U.S. Patent No. 6,345,330, filed Jan. 17, 2001, 5 pages.

Office Action for U.S. Patent No. 6,345,330, mailed Mar. 23, 2001, 6 pages.

Response to Office Action for U.S. Patent No. 6,345,330, filed Jul. 19, 2001, 5 pages.

Office Action for U.S. Appl. No. 09/642,628, mailed Apr. 5, 2001, 9 pages.

Office Action for U.S. Appl. No. 10/963,825, mailed Oct. 27, 2005, 25 pages.

Response for U.S. Appl. No. 10/963,825, filed Jan. 9, 2006, 22 pages.

Office Action for U.S. Appl. No. 10/963,825, mailed May 31, 2006, 29 pages.

Amendment Submitted with RCE for U.S. Appl. No. 10/963,825, filed Jul. 27, 2006, 29 pages.

Office Action for U.S. Appl. No. 10/963,825, mailed Oct. 20, 2006, 28 pages.

Appellants' Brief for U.S. Appl. No. 10/963,825, filed Jan. 8, 2007, 31 pages.

Revised Appellants' Brief for U.S. Appl. No. 10/963,825, filed Apr. 20, 2007, 34 pages.

Examiner's Answer for U.S. Appl. No. 10/963,825, mailed Aug. 8, 2007, 30 pages.

Reply Brief for U.S. Appl. No. 10/963,825, filed Sep. 4, 2007, 4 pages.

Decision on Appeal for U.S. Appl. No. 10/963,825, mailed Feb. 4, 2009, 13 pages.

Amendment Submitted with RCE for U.S. Appl. No. 10/963,825, filed Feb. 20, 2009, 24 pages.

Office Action for U.S. Appl. No. 10/963,825, mailed May 14, 2009, 5 pages.

Response for U.S. Appl. No. 10/963,825, filed May 22, 2009, 2 pages.

Office Action for U.S. Appl. No. 10/963,825, mailed Sep. 15, 2009, 14 pages.

Response for U.S. Appl. No. 10/963,825, filed Oct. 1, 2009, 7 pages.

Office Action for RE 41,294, mailed Nov. 16, 2007, 10 pages.

Response for RE 41,294, filed Dec. 20, 2007, 21 pages.

Office Action for RE 41,294, mailed Apr. 15, 2008, 10 pages.

Amendment Submitted with RCE for RE 41,294, filed May 27, 2008, 14 pages.

Supplemental Amendment Submitted with RCE for RE 41,294, filed Jul. 8, 2008, 12 pages.

Office Action for RE 41,294, mailed Sep. 16, 2008, 11 pages.

Response for RE 41,294, filed Oct. 30, 2008, 14 pages.

Supplemental Response for RE 41,294, filed Feb. 20, 2009, 13 pages.

Supplemental Response for RE 41,294, filed Aug. 17, 2009, 3 pages.

Examiner Interview Summary Record, mailed Jan. 15, 2009, 1 page.

Office Action for RE 41,076, mailed Jul. 13, 2007, 38 pages.

Response for RE 41,076, filed Sep. 26, 2007, 18 pages.

Office Action for RE 41,076, mailed Oct. 17, 2007, 55 pages.

Amendment Submitted with RCE for RE 41,076, filed Nov. 5, 2007, 19 pages.

Office Action for RE 41,076, mailed Feb. 11, 2008, 62 pages.

Response for RE 41,076, filed Apr. 7, 2008, 18 pages.

Office Action for RE 41,076, mailed Jun. 9, 2008, 25 pages.

Amendment Submitted with RCE for RE 41,076, filed Dec. 8, 2008, 44 pages.



**US RE43,171 E**

Page 12

Office Action for RE 41,076, mailed Dec. 30, 2008, 8 pages.  
 Response for RE 41,076, filed Jan. 16, 2009, 14 pages.  
 Amendment Submitted with RCE for RE 41,076, filed Aug. 4, 2009, 2 pages.  
 Examiner Interview Summary Record, mailed Feb. 24, 2009, 4 pages.  
 Applicant Summary of Interview, filed Mar. 24, 2009, 1 page.  
 Examiner Interview Summary Record, mailed Sep. 22, 2009, 5 pages.  
 Office Action for U.S. Appl. No. 12/322,858, mailed Mar. 4, 2010, 24 pages.  
 Response for U.S. Appl. No. 12/322,858, filed Jun. 4, 2010, 15 pages.  
 Office Action for U.S. Appl. No. 12/322,858, mailed Jun. 25, 2010, 22 pages.  
 Response for U.S. Appl. No. 12/322,858, filed Oct. 25, 2010, 12 pages.  
 Office Action for U.S. Appl. No. 12/577,074, mailed Apr. 13, 2010, 7 pages.  
 Response for U.S. Appl. No. 12/577,074, filed Jul. 13, 2010, 3 pages.  
 Office Action for U.S. Appl. No. 12/577,074, mailed Nov. 10, 2010, 6 pages.  
 Office Action for U.S. Appl. No. 09/312,199, mailed Mar. 26, 2003, 5 pages.  
 Response for U.S. Appl. No. 09/312,199, filed Jun. 11, 2003, 5 pages.  
 Office Action for RE 41,092, mailed Sep. 17, 2008, 8 pages.  
 Response for RE 41,092, filed Oct. 27, 2008, 27 pages.  
 Examiner's Amendment for RE 41,092, mailed Nov. 4, 2009, 4 pages.  
 Office Action for U.S. Appl. No. 11/545,056, mailed Mar. 12, 2010, 26 pages.  
 Response for U.S. Appl. No. 11/545,056, filed Jun. 14, 2010, 18 pages.  
 Office Action for U.S. Appl. No. 12/561,138, mailed Sep. 29, 2010, 4 pages.  
 Request for Ex Parte Reexamination of U.S. Patent No. 6,216,185, Control No. 90/010,816, filed Jan. 8, 2010, 39 pages.  
 Request for Ex Parte Reexamination of U.S. Patent No. 6,216,185, Control No. 90/010,816, filed Jan. 8, 2010, Exhibit AA to Request Claim Charts with respect to the Hitachi '953 for Anticipation and Obviousness, 136 pages.  
 Request for Ex Parte Reexamination of U.S. Patent No. 6,216,185, Control No. 90/010,816, filed Jan. 8, 2010, Exhibit BB Claim Charts with respect to Kobayashi for Anticipation and Obviousness, 128 pages.  
 Request for Ex Parte Reexamination of U.S. Patent No. 6,216,185, Control No. 90/010,816, filed Jan. 8, 2010, Exhibit CC Claim Charts with respect to Byte for Anticipation and Obviousness, 122 pages.  
 Request for Ex Parte Reexamination of U.S. Patent No. 6,216,185, Control No. 90/010,816, filed Jan. 8, 2010, Exhibit DD Claim Charts with respect to the Hitachi '675 for Anticipation and Obviousness, 119 pages.  
 Office Action in Ex Parte Reexamination of U.S. Patent No. 6,216,185, Control No. 90/010,816, mailed Jul. 27, 2010, 103 pages.  
 Patent Owner's Response to Office Action in Ex Parte Reexamination of U.S. Patent No. 6,216,185, Control No. 90/010,816, filed Sep. 27, 2010, 55 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, filed Dec. 2, 2009, 44 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, filed Dec. 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, Nov. 24, 2009, 3 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit AA, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed Jan. 5, 2010, 109 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit BB, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed Jan. 5, 2010, 91 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit CC, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed Jan. 5, 2010, 85 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit DD, Claim Charts with respect to the Origin2000 Manual for Obviousness, filed Jan. 5, 2010, 72 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, Replacement Exhibit EE, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed Jan. 5, 2010, 107 pages.  
 Office Action in Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, mailed May 26, 2010, 39 pages.  
 Patent Owner's Response to Office Action in Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, filed Jul. 27, 2010, 41 pages.  
 Patent Owner's Response to Office Action in Inter Partes Reexamination of U.S. Patent No. 6,718,415, Control No. 95/001,276, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed Jul. 27, 2010, 29 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, filed Feb. 9, 2010, 33 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, filed Dec. 2, 2009, Exhibit O, Declaration Under 37 CFR 1.132 of Vincent P. Conroy, Nov. 24, 2009, 3 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, Exhibit AA, Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed Feb. 9, 2010, 164 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, Exhibit BB, Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed Feb. 9, 2010, 158 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed Feb. 9, 2010, 167 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, Exhibit DD, Claim Charts with respect to the Eversys for Obviousness, filed Feb. 9, 2010, 111 pages.  
 Office Action in Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, mailed Jul. 6, 2010, 83 pages.  
 Patent Owner's Response to Office Action in Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, filed Sep. 3, 2010, 52 pages.  
 Patent Owner's Response to Office Action in Inter Partes Reexamination of U.S. Patent No. 7,099,981, Control No. 95/001,310, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed Sep. 3, 2010, 63 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, filed Mar. 19, 2010, 35 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 1), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed Mar. 19, 2010, 186 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, Exhibit AA (Part 2), Claim Charts with respect to Gallagher for Anticipation and Obviousness, filed Mar. 19, 2010, 161 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 1), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed Mar. 19, 2010, 139 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, Exhibit BB (Part 2), Claim Charts with respect to QuantumNet for Anticipation and Obviousness, filed Mar. 19, 2010, 128 pages.  
 Request for Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, Exhibit CC, Claim Charts with respect to Chatcom for Anticipation and Obviousness, filed Mar. 19, 2010, 68 pages.  
 Office Action in Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, mailed Jun. 24, 2010, 86 pages.  
 Patent Owner's Response to Office Action in Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, filed Aug. 24, 2010, 45 pages.

**US RE43,171 E**

Page 13

Patent Owner's Response to Office Action in Inter Partes Reexamination of U.S. Patent No. 7,146,446, Control No. 95/001,328, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed Sep. 3, 2010, 61 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,328,297, Control No. 95/001,336, filed Apr. 19, 2010, 33 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,328,297, Control No. 95/001,336, Exhibit AA, Claim Charts with respect to Gallagher for Obviousness, filed Apr. 19, 2010, 131 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,328,297, Control No. 95/001,336, Exhibit BB, Claim Charts with respect to QuantumNet for Obviousness, filed Apr. 19, 2010, 139 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,328,297, Control No. 95/001,336, Exhibit CC, Claim Charts with respect to Chatcom for Obviousness, filed Apr. 19, 2010, 114 pages.

Office Action in Inter Partes Reexamination of U.S. Patent No. 7,328,297, Control No. 95/001,336, mailed Aug. 4, 2010, 95 pages.

Patent Owner's Response to Office Action in Inter Partes Reexamination of U.S. Patent No. 7,328,297, Control No. 95/001,336, filed Oct. 4, 2010, 49 pages.

Patent Owner's Response to Office Action in Inter Partes Reexamination of U.S. Patent No. 7,328,297, Control No. 95/001,336, Exhibit A, Declaration of William Henry Mangione-Smith under 37 C.F.R. 1.132, filed Oct. 4, 2010, 61 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,415, Control No. 95/001,424, filed Aug. 25, 2010, 34 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,415, Control No. 95/001,424, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed Aug. 25, 2010, 114 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,415, Control No. 95/001,424, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed Aug. 25, 2010, 92 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,415, Control No. 95/001,424, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed Aug. 25, 2010, 121 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,415, Control No. 95/001,424, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed Aug. 25, 2010, 99 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,415, Control No. 95/001,424, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed Aug. 25, 2010, 91 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,415, Control No. 95/001,424, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed Aug. 25, 2010, 94 pages.

Office Action in Inter Partes Reexamination of U.S. Patent No. 7,363,415, Control No. 95/001,424, mailed Nov. 1, 2010, 75 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,376,779, Control No. 95/001,475, filed Oct. 27, 2010, 35 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,376,779, Control No. 95/001,475, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed Oct. 27, 2010, 128 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,376,779, Control No. 95/001,475, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed Oct. 27, 2010, 153 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,376,779, Control No. 95/001,475, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed Oct. 27, 2010, 108 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,376,779, Control No. 95/001,475, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed Oct. 27, 2010, 112 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,376,779, Control No. 95/001,475, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed Oct. 27, 2010, 112 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,376,779, Control No. 95/001,475, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed Oct. 27, 2010, 118 pages.

Office Action in Inter Partes Reexamination of U.S. Patent No. 7,376,779, Control No. 95/001,475, mailed Dec. 20, 2010, 105 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,416, Control No. 95/001,476, filed Oct. 27, 2010, 37 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,416, Control No. 95/001,476, Exhibit AA, Claim Charts with respect to Gallagher and Other References for Obviousness, filed Oct. 27, 2010, 70 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,416, Control No. 95/001,476, Exhibit AB, Claim Charts with respect to Gallagher and Other References for Obviousness, filed Oct. 27, 2010, 64 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,416, Control No. 95/001,476, Exhibit BA, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed Oct. 27, 2010, 64 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,416, Control No. 95/001,476, Exhibit BB, Claim Charts with respect to QuantumNet and Other References for Obviousness, filed Oct. 27, 2010, 71 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,416, Control No. 95/001,476, Exhibit CA, Claim Charts with respect to Chatcom and Other References for Obviousness, filed Oct. 27, 2010, 64 pages.

Request for Inter Partes Reexamination of U.S. Patent No. 7,363,416, Control No. 95/001,476, Exhibit CB, Claim Charts with respect to Chatcom and Other References for Obviousness, filed Oct. 27, 2010, 67 pages.

Office Action in Inter Partes Reexamination of U.S. Patent No. 7,363,416, Control No. 95/001,476, mailed Dec. 6, 2010, 63 pages.

"Defendants' Amended Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 18 pages.

"Exhibit A (Asserted Claims)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 2 pages.

"Exhibit B—Table 1," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 75 pages.

"Exhibit C," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 2 pages.

"Exhibit D," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 106 pages.

"Exhibit E," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 2 pages.

"Invalidity Chart for Base Reference IBM 8260," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 53 pages.

"Invalidity Chart for Base Reference IBM 8265," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 56 pages.

"Invalidity Chart for Base Reference U.S. Patent No. 4,453,215 (Reid)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 56 pages.

"Invalidity Chart for Base Reference Origin2000," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 56 pages.

"Invalidity Chart for Base Reference QuantumNet," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 49 pages.

## US RE43,171 E

Page 14

"Invalidity Chart for Base Reference U.S. Patent No. 6,564,274 (Heath)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 57 pages.

"Invalidity Chart for Base Reference U.S. Patent No. 5,577,205," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 60 pages.

"Invalidity Chart for Base Reference U.S. Patent No. 5,802,391," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 61 pages.

"Invalidity Chart for Base Reference U.S. Patent No. 6,715,100," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 64 pages.

"Invalidity Chart for Base Reference Cubix BC/Density," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 64 pages.

"Invalidity Chart for Base Reference JP6-289956," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 62 pages.

"Invalidity Chart for Base Reference Gallagher 068 and Gallagher 503," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 108 pages.

"Invalidity Chart for Base Reference Compaq ProLiant Cluster," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 81 pages.

"Invalidity Chart for Base Reference U.S. Patent No. 5,325,517 to Baker et al. (Appendix 1, Exhibit 15)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 59 pages.

"Invalidity Chart for Japanese Patent Application H7-64672 (Toshiba '672)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 55 pages.

"Invalidity Chart for Base Reference ChatCom," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 52 pages.

"Invalidity Chart for Base Reference Ziatech Corp. Ketris 9000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 68 pages.

"Invalidity Chart for Base Reference Ziatech STD 32 Star System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 62 pages.

"Invalidity Chart for Base Reference U.S. Patent No. 7,339,786 (Bottom et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 57 pages.

"Invalidity Chart for Base References RLX Patents, U.S. Patent Nos. 6,747,878, 6,411,506, 6,325,636, 6,757,748, and 6,985,967 (Hipp et al.)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 58 pages.

"Invalidity Chart for Base Reference Network Engines P6000 Server," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 59 pages.

"Invalidity Chart for Base Reference Eversys 8000 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 60 pages.

"Invalidity Chart for Base Reference Eversys CAPserver," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 59 pages.

"Invalidity Chart for Base Reference U.S. 5,809,262," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 62 pages.

"Invalidity Chart for Base Reference WhiteCross 9800 System," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 62 pages.

"Invalidity Chart for Base Reference U.S. 5,339,408," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 61 pages.

"Invalidity Chart for Base Reference Tyuluman 536," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 76 pages.

"Invalidity Chart for Base Reference Hong 737," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 77 pages.

"Invalidity Chart for Base Reference U.S. 5,436,857 (Nelson)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 6 pages.

"Invalidity Chart for Base Reference U.S. 5,999,952 (Jenkins)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 6 pages.

"Invalidity Chart for Base Reference U.S. 5,608,608 (Flint)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 6 pages.

"Invalidity Chart for Base Reference U.S. 5,978,821 (Freemy)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 6 pages.

"Invalidity Chart for Base Reference WO 92/18924 (Wallsten)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 6 pages.

"Invalidity Chart for Base Reference Ergo Moby Brick," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 5 pages.

"Invalidity Chart for Base Reference U.S. Patent No. 5,463,742 (Kobayashi)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 5 pages.

"Invalidity Chart for Base Reference Japanese Patent Application Publication H6-289953 (Hitachi)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 5 pages.

"Invalidity Chart for Base Reference Japanese Patent Application Publication H7-84675 (Hitachi)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 5 pages.

"Invalidity Chart for Base Reference U.S. Patent No. 5,187,645 (Spalding)," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 6 pages.

"Defendants' Notice of Errata Relating to Defendants' P.R. 3-3 Invalidity Contentions," submitted by the Defendants in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED on Mar. 1, 2010, 14 pages.

"Memorandum Opinion and Order Construing Claim Terms," Issued by the U.S. District Court for the Eastern District of Texas, Tyler Division, Case No. 6:09-cv-148-LED, Document 602, Feb. 3, 2011, 12 pgs.

\* cited by examiner

U.S. Patent

Feb. 7, 2012

Sheet 1 of 14

US RE43,171 E

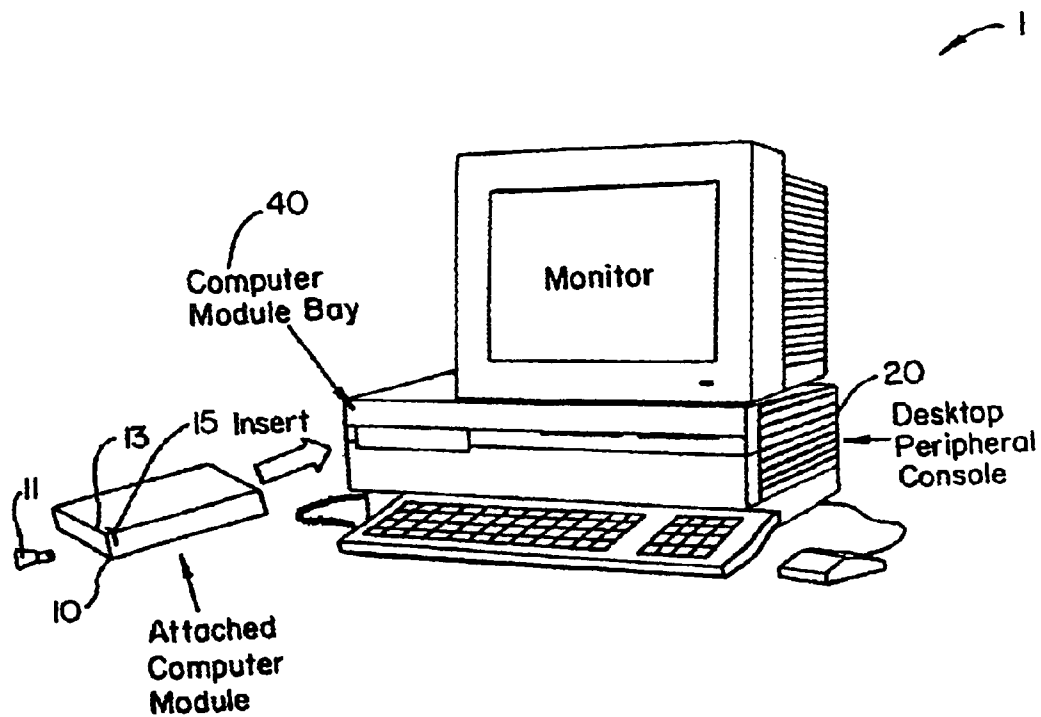


FIG. 1

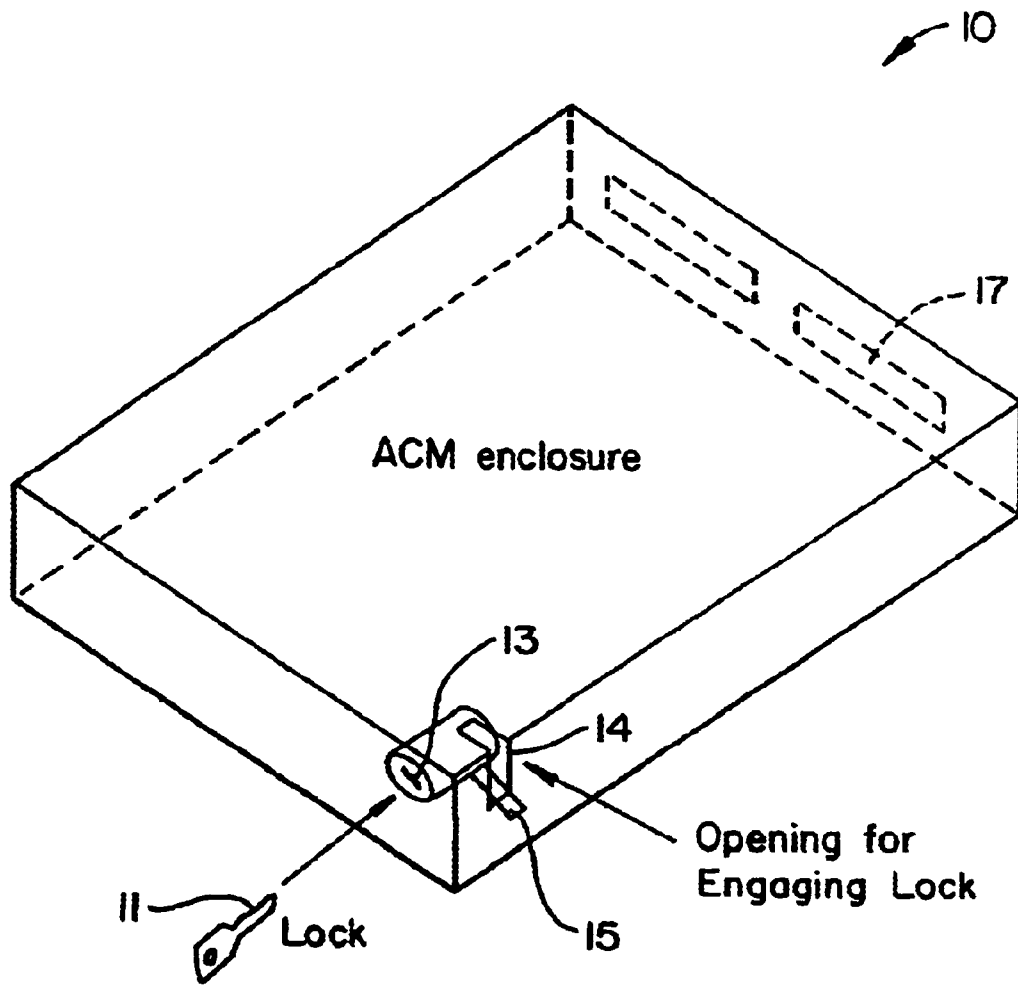


U.S. Patent

Feb. 7, 2012

Sheet 2 of 14

US RE43,171 E



**FIG 2**

U.S. Patent

Feb. 7, 2012

Sheet 3 of 14

US RE43,171 E

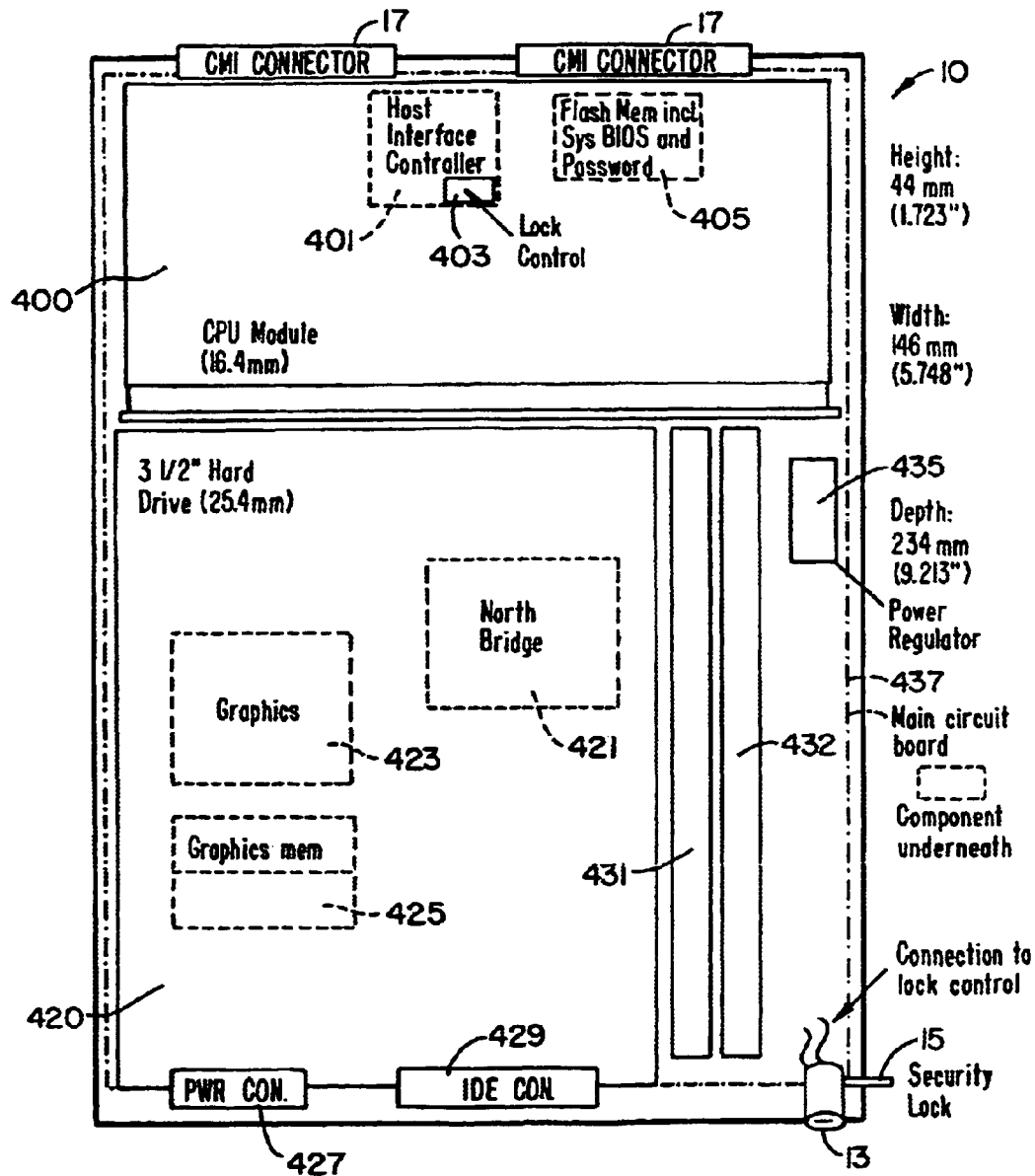
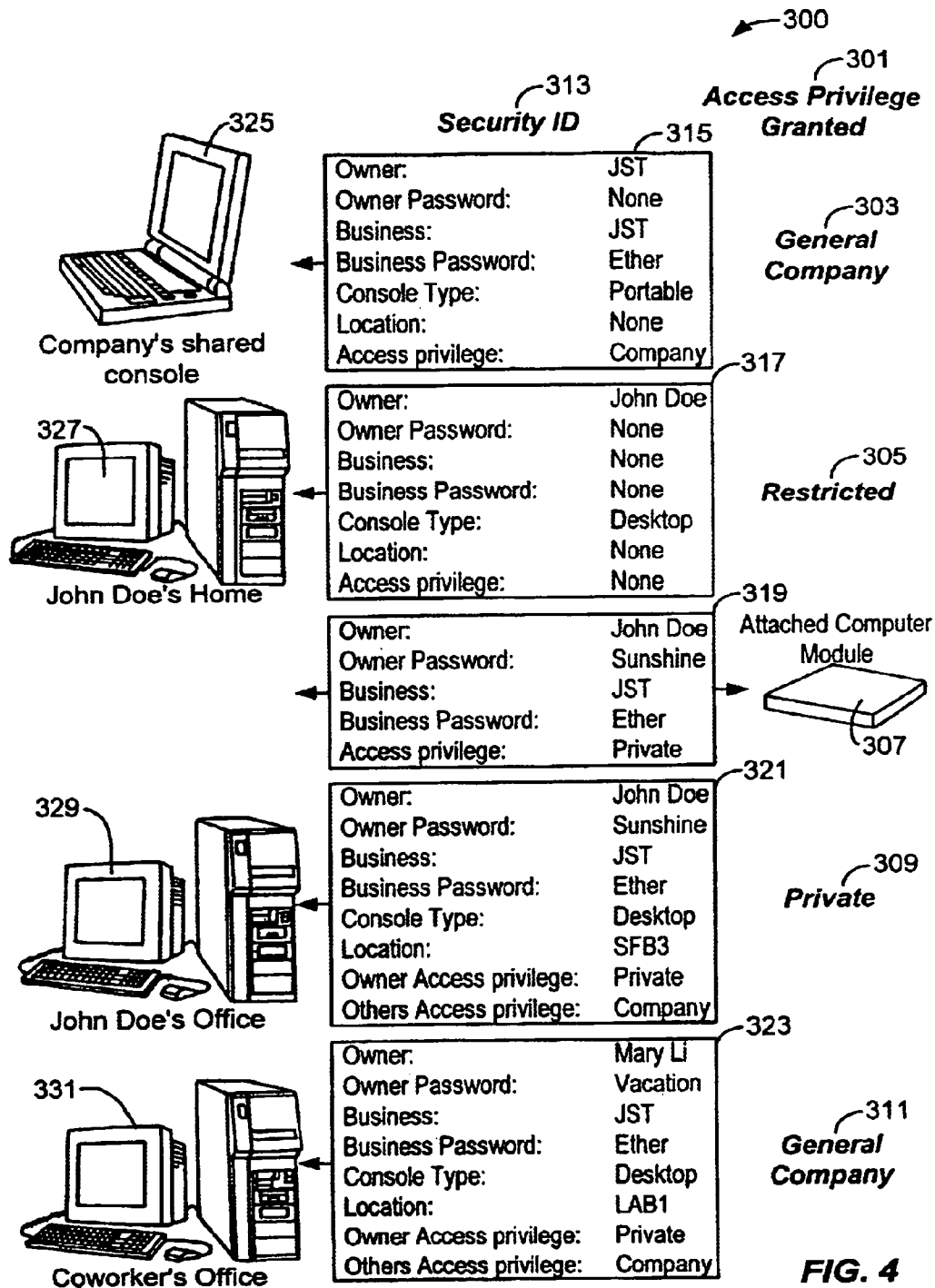


FIG. 3



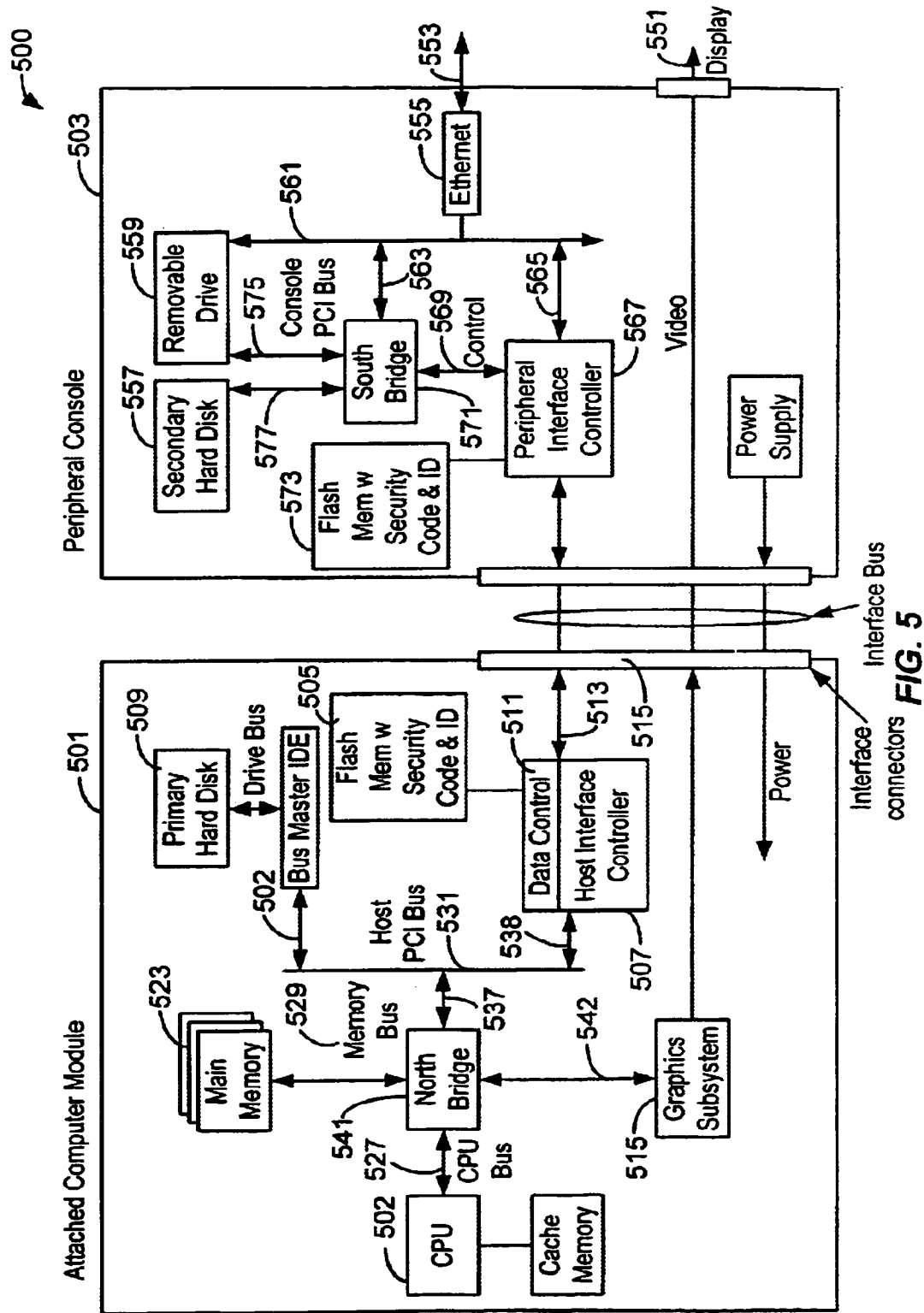


FIG. 5



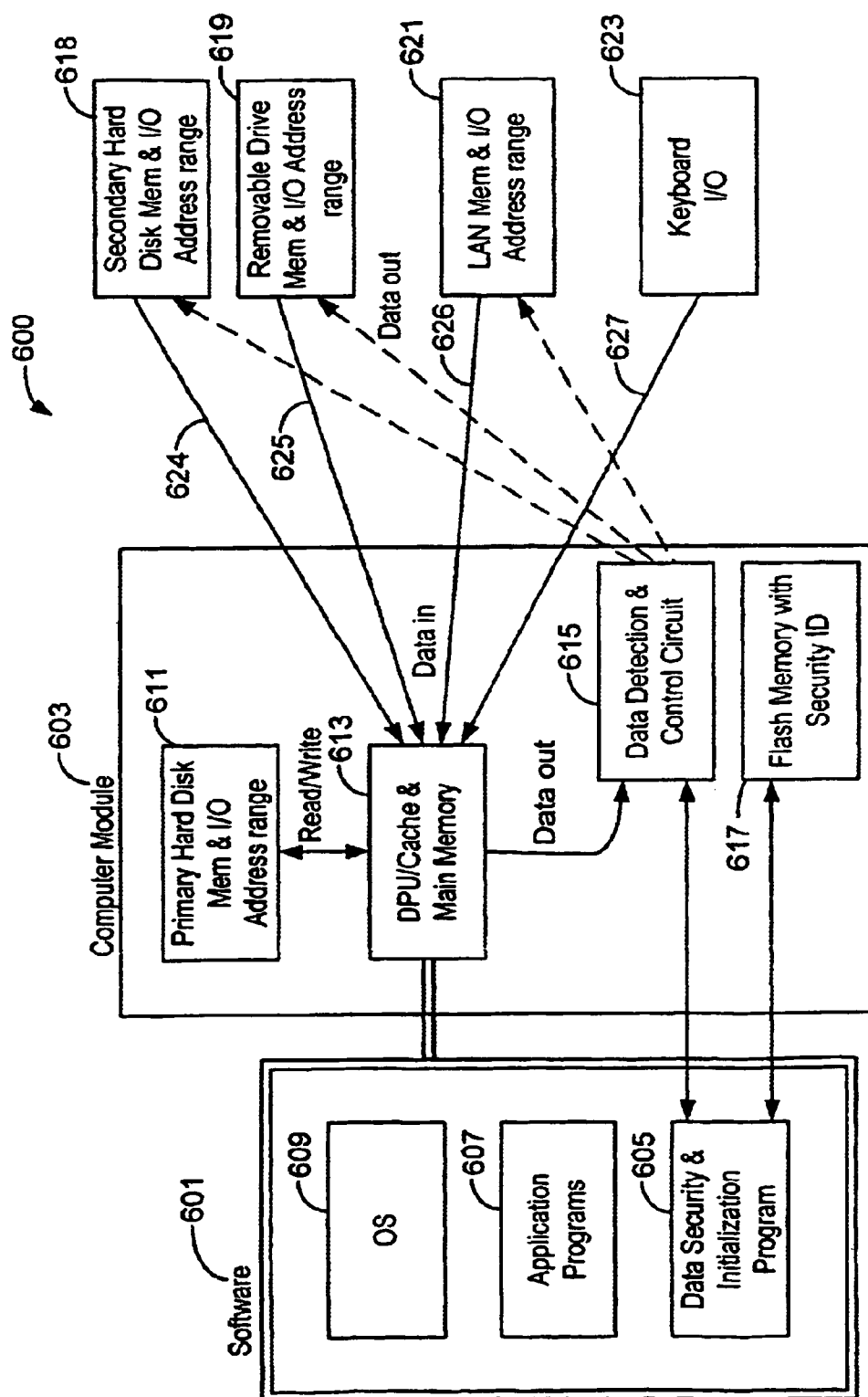


FIG. 6

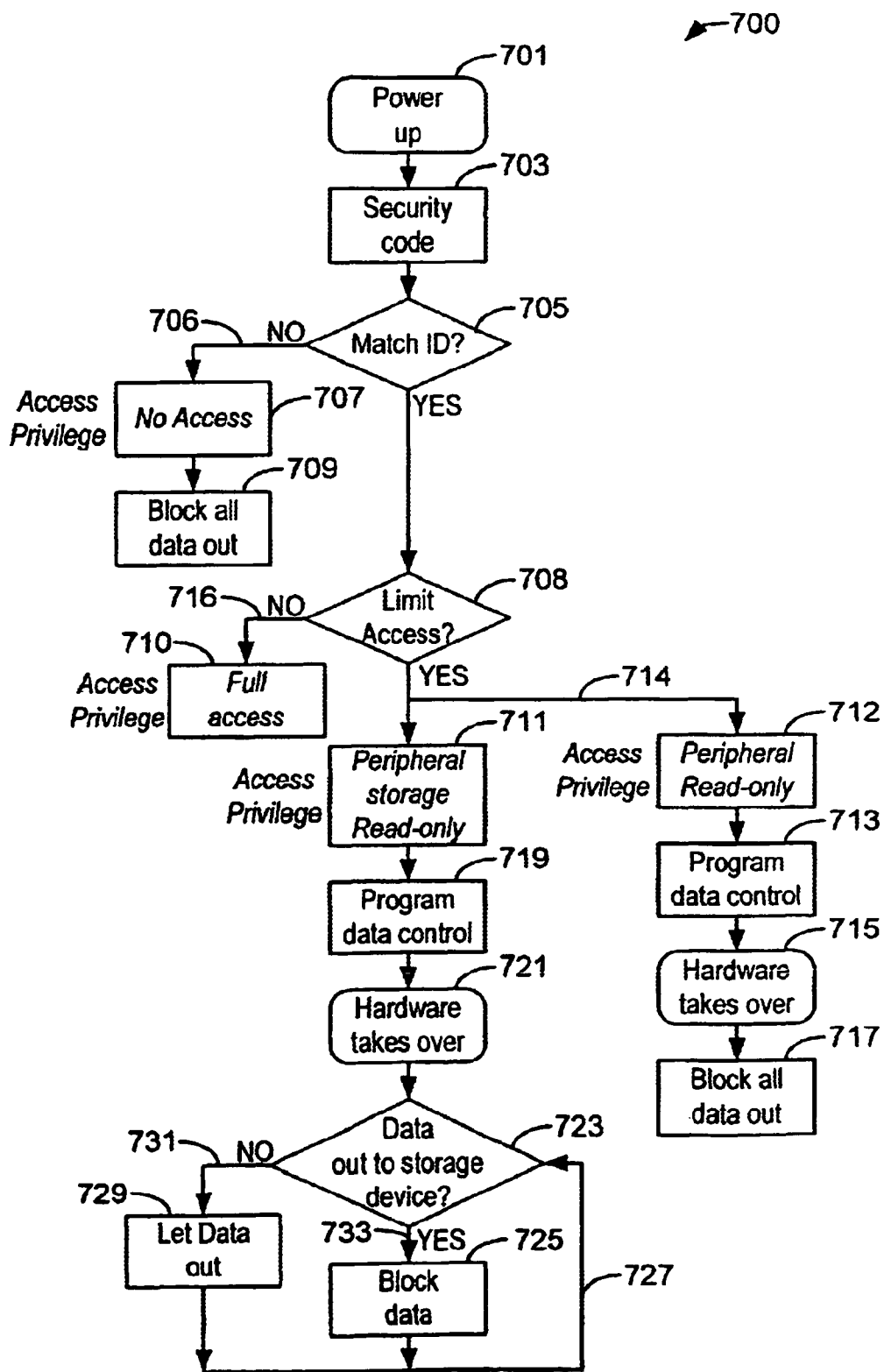


FIG. 7

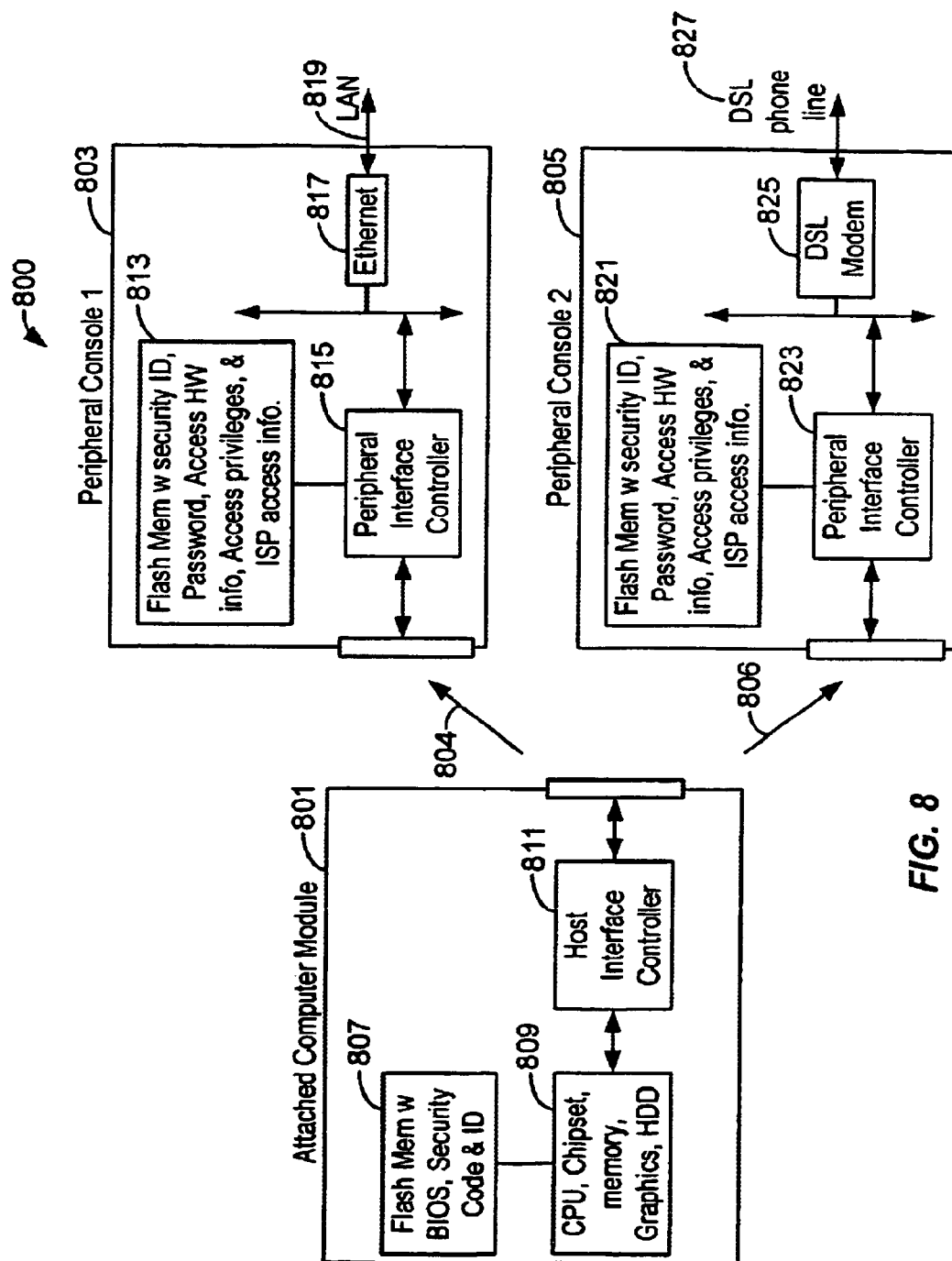


FIG. 8

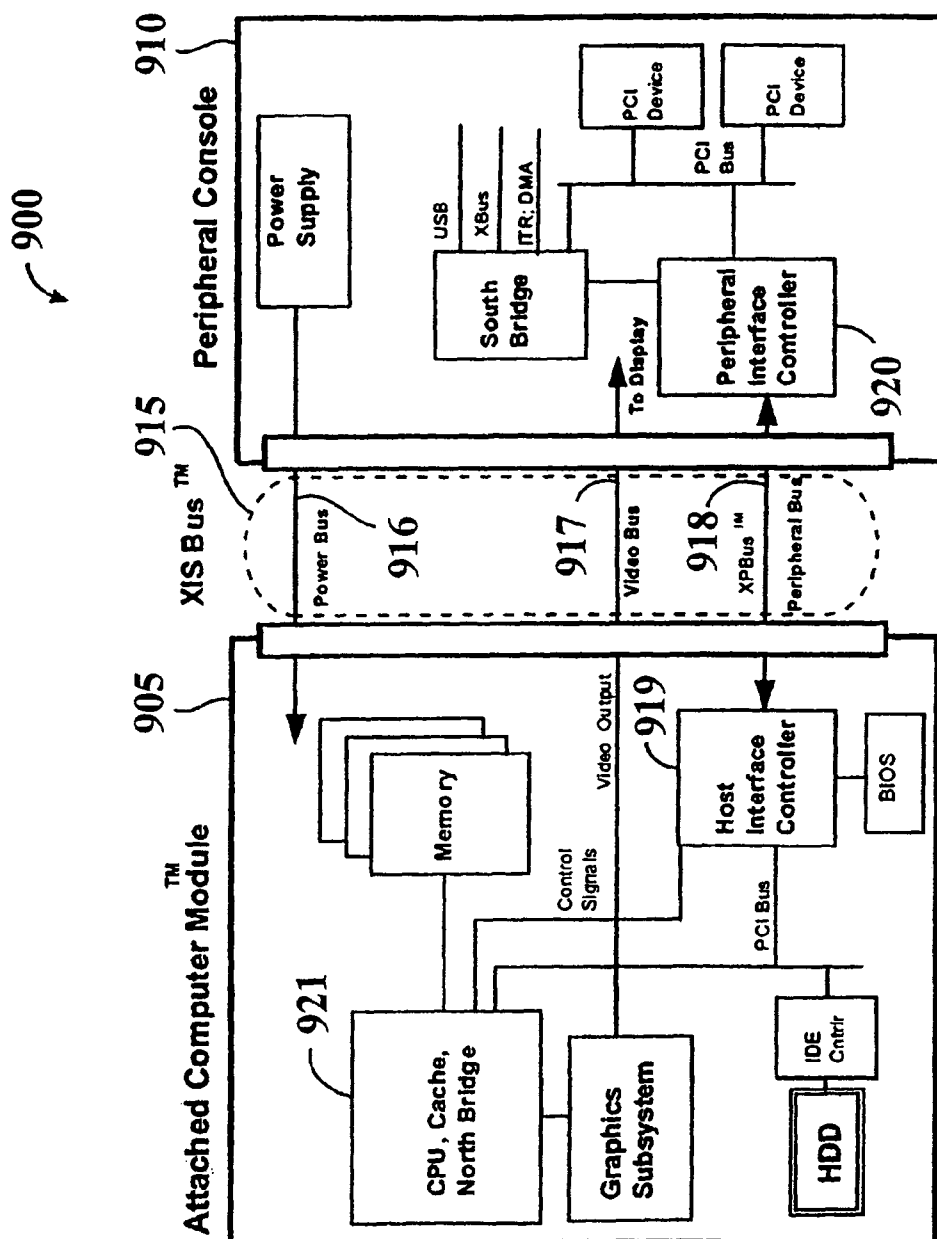


FIG. 9



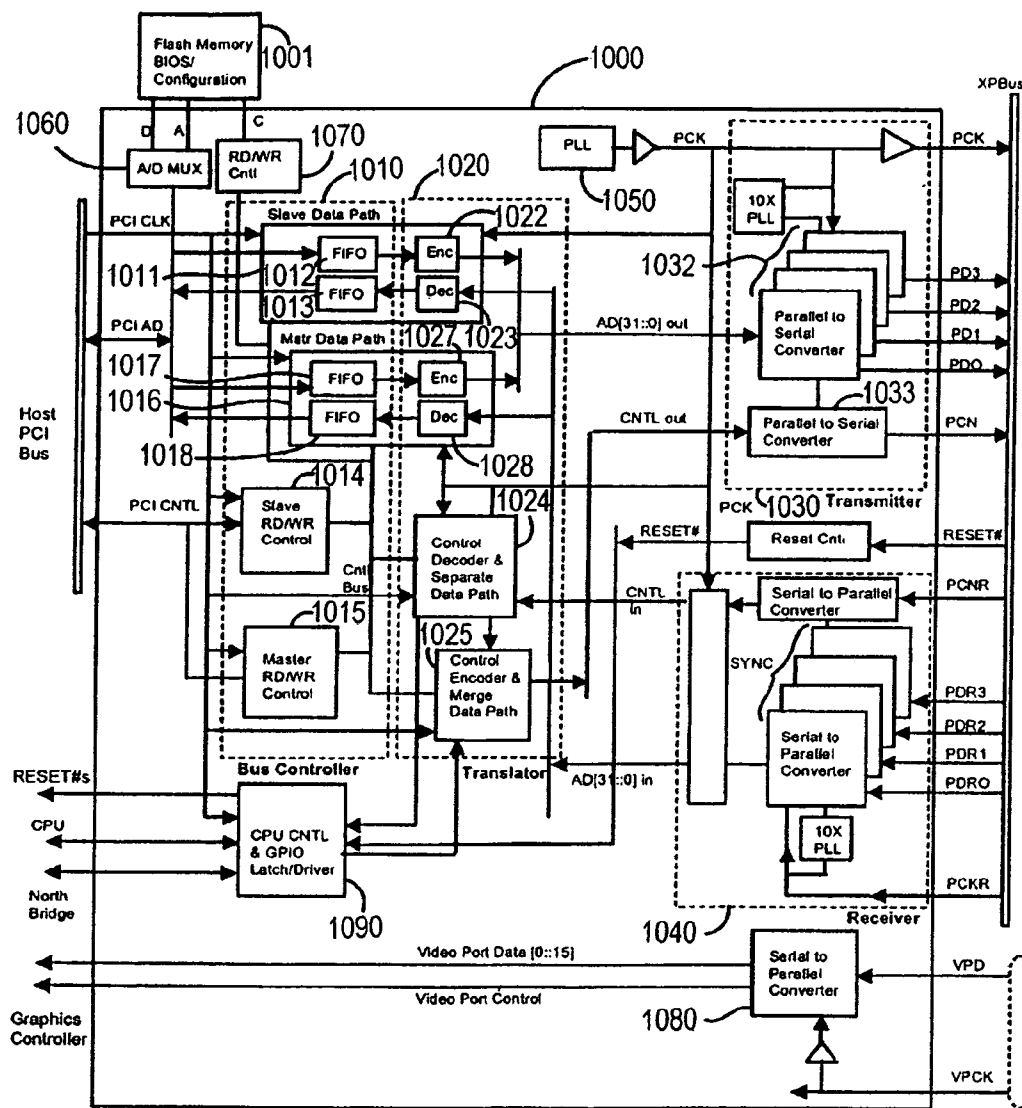


FIG. 10

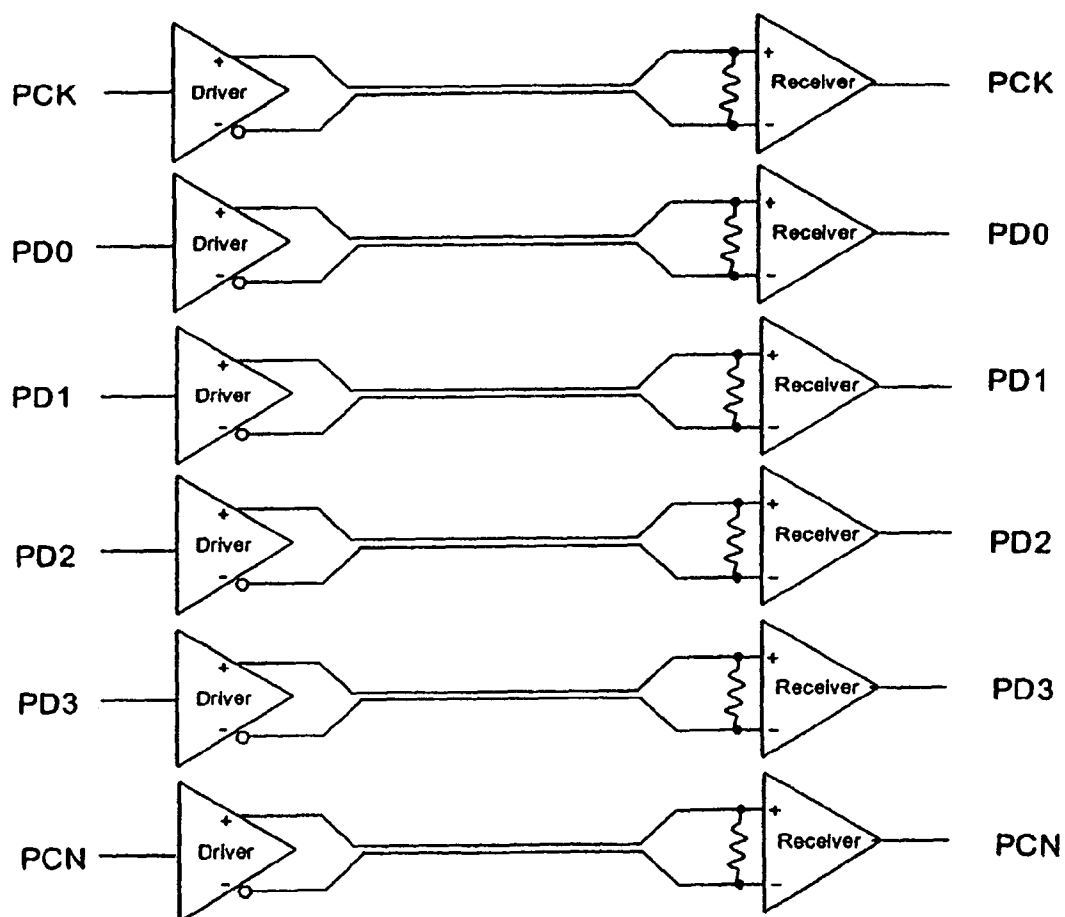


FIG. 11

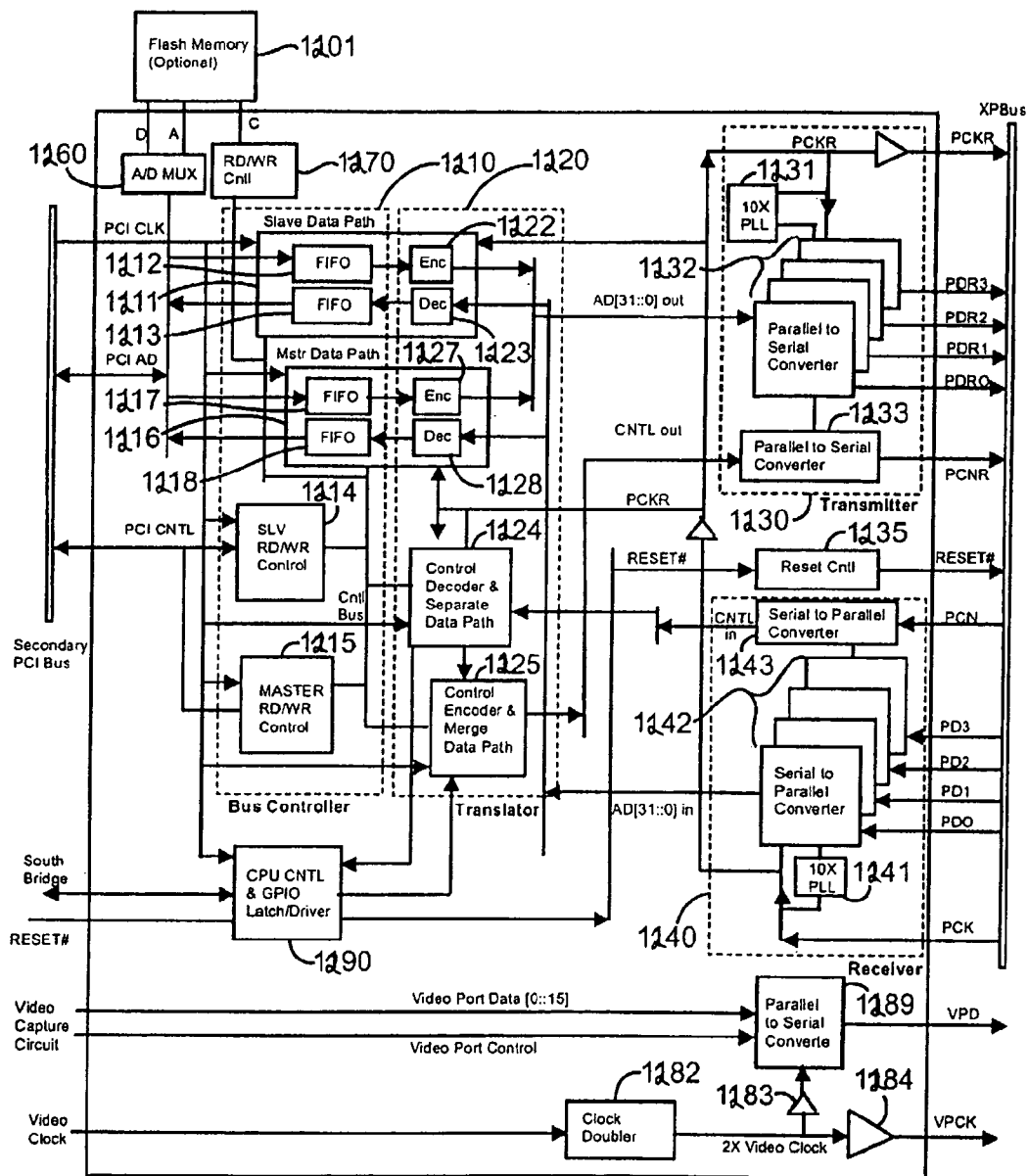


FIG. 12

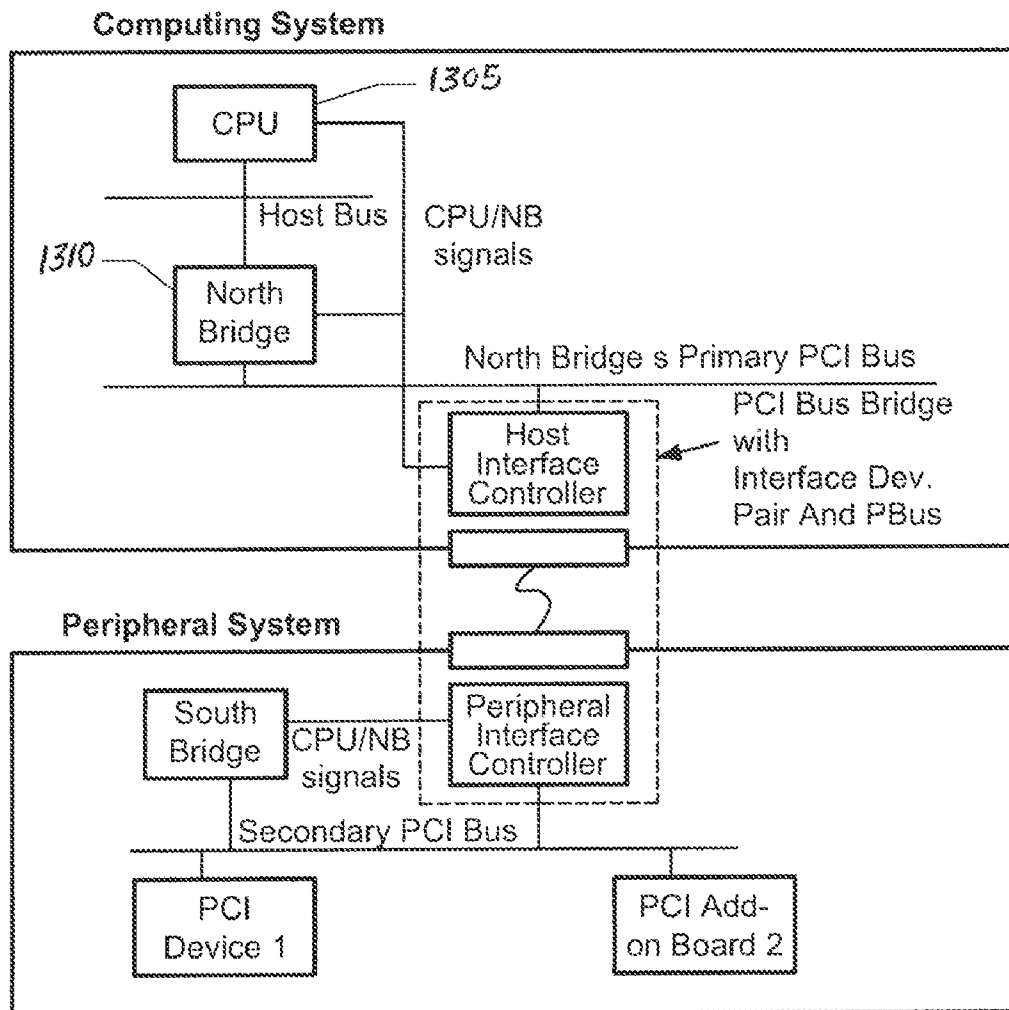


FIGURE 13

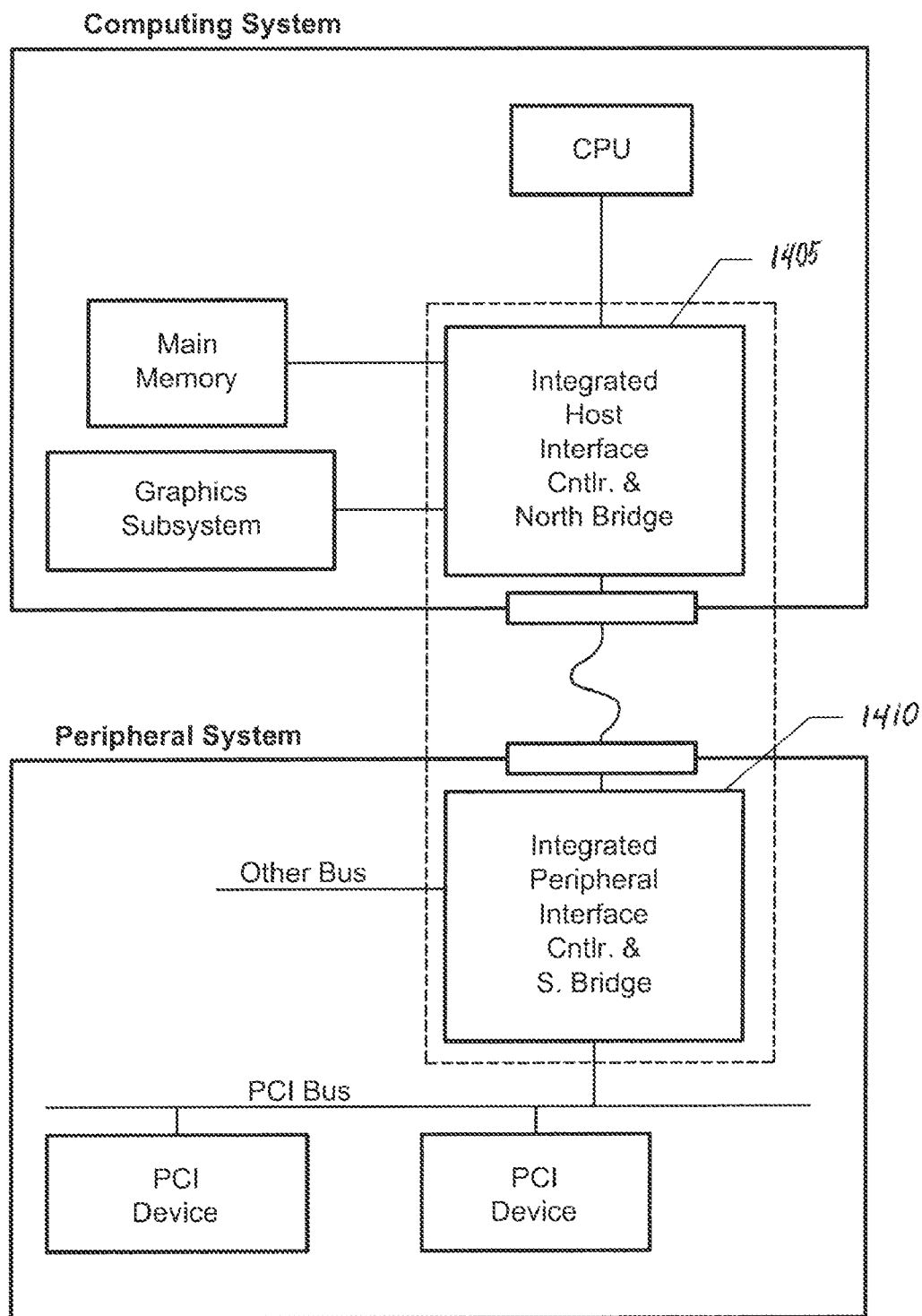


FIGURE 14



## US RE43,171 E

1

DATA SECURITY METHOD AND DEVICE  
FOR COMPUTER MODULES

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

*Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 6,643,777. The reissue applications are U.S. application Ser. Nos. 11/056,604 (a parent reissue application and now U.S. Pat. No. Re. 41,092), 11/545,056 (the present application, which is a continuation reissue of the parent reissue application), and 12/561,138 (which is a continuation reissue of the parent reissue application).*

*This application is a continuation reissue of U.S. application Ser. No. 11/056,604, which is a reissue of U.S. Pat. No. 6,643,777, which are incorporated herein by reference.*

## BACKGROUND OF THE INVENTION

The present invention relates to computing devices. More particularly, the present invention provides a method and device for securing a personal computer or set-top box. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive including memory in the giga-byte range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 19 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many

2

limitations. These computing devices have expensive display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals the are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use. The docking station typically includes a separate monitor, keyboard, mouse, and the like and is generally incompatible with other desktop PCs. The docking station is also generally not compatible with portable computers of other vendors. Another drawback to this approach is that the portable computer typically has lower performance and functionality than a conventional desktop PC. For example, the processor of the portable is typically much slower than processors in dedicated desktop computers, because of power consumption and heat dissipation concerns. As an example, it is noted that at the time of drafting of the present application, some top-of-the-line desktops include 400 MHz processors, whereas top-of-the-line notebook computers include 266 MHz processors.

Another drawback to the docking station approach is that the typical cost of portable computers with docking stations can approach the cost of having a separate portable computer and a separate desktop computer. Further, as noted above, because different vendors of portable computers have proprietary docking stations, computer users are held captive by their investments and must rely upon the particular computer vendor for future upgrades, support, and the like.

To date, most personal computers provide data file security through software only. A wide variety of removable storage media are available for a personal computer. These removable

## US RE43,171 E

3

media do not provide any access security protection in hardware. Data encryption program often must be used for protection. Such program is cumbersome to handle for the user requiring extra cost and time. Data encryption is more commonly used for communication over an unprotected network or the Internet. Having a large number of frequently used files managed by encryption software is not practical. Without software security program, any file can be read and copied illegally from a hard disk drive on a PC or any removable media.

PC architecture generally allows freedom of data flow between memory and peripheral devices within the allowed memory and I/O address spaces. In conventional PC architecture, a peripheral bus, i.e. PCI bus, is used to control all data transactions among peripheral devices. PCI bus allows any device to be a bus master and perform data transaction with another device. Also when a software program is in control, it can move data between any two devices. There is no hardware or protocol security mechanism on a standard peripheral bus such as PCI Bus to detect or block data transactions. Operating system may have individual files read or write protected. These types of special security feature require significant additional user interaction to control. This is too cumbersome for a typical user to manage. There is no mechanism in current PCs to allow access to the primary hard disk drive and yet prevent copying of its content. The conventional PC is a single machine that does not have a mechanism to perform security ID matching in hardware.

Thus, what is needed are computer systems that provide improved security features to prevent illegal or unauthorized access to information.

## SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for securing a computer module in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a computer module bay (CMB) within a peripheral console to form a functional computer. A security program reads an identification number in a security memory device to determine a security level of the ACM according to one embodiment.

In a specific embodiment, the present invention provides a system for secured information transactions. The system has a console (e.g., computer housing) comprising a peripheral controller housed in the console; and a security memory device (e.g., flash memory device) coupled to the peripheral controller. The system also has an attached computer module (i.e., a removable module with memory and microprocessor) coupled to the console. The attached computer module has a host interface controller housed within the attached computer module to interface to the security memory device through the peripheral controller.

In an alternative embodiment, the present invention provides a security protection method for a computer module. The method includes steps or acts of inserting the computer module into a console. Once the module has been inserted, the method initiates a security program in the module to read a security identification of the console and to read a security identification of the computer module. Based upon a relationship of the console identification and the computer module identification, a predetermined security status is determined from, for example, a look up table or the like. The method then

4

selects the predetermined security status, which can be one of many. The method then operates the computer module based upon the security status.

In a further alternative embodiment, the present invention provides a method for identifying a user for a computer module. The method includes inserting a computer module into a console; and initiating a security program in memory of the computer module. The method prompts a plurality of input fields corresponding to respective input information on a user interface to be provided by a user of the computer module. Next, the method inputs the input information into the user interface of the computer module. The input information includes a user (e.g., owner) name, a user (e.g., owner) password, a business name, a business password, and a location.

Still further, the present invention provides a system for secured information transactions, e.g., data security, electronic commerce, private communications. The system includes a console comprising a peripheral controller housed in the console. A user identification input device (e.g., keyboard, retinal reader, finger print reader, voice recognition unit) is coupled to the peripheral controller. The user identification input device is provided for user identification data of the user. The system has an attached computer module coupled to the console. The attached computer module has a security memory device (e.g., flash memory device) stored with the user identification data.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached FIGS.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified diagram of a computer module according to an embodiment of the present invention;

FIG. 3 is a simplified top-view diagram of a computer module according to an embodiment of the present invention;

FIG. 4 is a simplified illustration of security systems according to embodiments of the present invention;

FIG. 5 is a simplified diagram of a computer module in a console according to an embodiment of the present invention;

FIG. 6 is a simplified diagram of a security method for a module according to an embodiment of the present invention; and

FIG. 7 is a simplified diagram of a method according to an embodiment of the present invention.

FIG. 8 is a simplified diagram of a system 800 according to an alternative embodiment of the present application.

FIG. 9 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

## US RE43,171 E

5

FIG. 11 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 12 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 13 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 14 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

#### DESCRIPTION OF THE SPECIFIC EMBODIMENTS

FIG. 1 is a simplified diagram of a computer system 1 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 1 includes an attached computer module (i.e., ACM) 10, a desktop console 20, among other elements. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

In the present embodiment, ACM 10 includes computer components, as will be described below, including a central processing unit ("CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) 40 is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to ACM 10. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending U.S. patent application Ser. Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998 commonly assigned, and hereby incorporated by reference for all purposes.

In a preferred embodiment, the present system has a security system, which includes a mechanical locking system, an electrical locking system, and others. The mechanical locking system includes at least a key 11. The key 11 mates with key hole 13 in a lock, which provides a mechanical latch 15 in a closed position. The mechanical latch, in the closed position, mates and interlocks the ACM to the computer module bay. The mechanical latch, which also has an open position, allows the ACM to be removed from the computer module bay. Further details of the mechanical locking system are shown in the FIG. below.

FIG. 2 is, a simplified diagram of a computer module 10 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous FIG. for easy reading. The computer module 10 includes key 11, which is insertable into keyhole 13 of the lock. The lock has at least two position, including a latched or closed position and an unlatched or open position. The latched position secures the ACM to the computer module bay. The unlatched or open position allows the ACM to be inserted into or removed from the computer bay module. As shown, the ACM also has a slot or opening 14, which allows the latch to move into and out of the ACM. The ACM also has

6

openings 17 in the backside for an electrical and/or mechanical connection to the computer module bay, which is connected to the console.

FIG. 3 is a simplified top-view diagram 10 of a computer module for computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 10, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module 400, and a second portion, which includes a hard drive module 420. A common printed circuit board 437 houses these modules and the like. Among other features, the ACM includes the central processing unit module 400 with a cache memory 405, which is coupled to a north bridge unit 421, and a host interface controller 401. The host interface controller includes a lock control 403. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 17. Here, the CPU module is spatially located near connector 17.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller 401 is coupled to BIOS/flash memory 405. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 403 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module 420. Among other elements, the hard drive module includes north bridge 421, graphics accelerator 423, graphics memory 425, a power controller 427, an IDE controller 429, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface ("PCI") bus 431, 432. A power regulator 435 is disposed near the PCI bus.

In a specific embodiment, north bridge unit 421 often couples to a computer memory, to the graphics accelerator 423, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 423 typically couples to a graphics memory 423, and other elements. IDE controller 429 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, USB, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit 420 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT,



## US RE43,171 E

7

MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 420 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

In a specific embodiment, the present invention provides a file and data protection security system and method for a removable computer module or ACM. ACM contains the primary hard disk drive (HDD) where the operating system, application programs, and data files reside. The security system is used to prevent illegal access and copying of any file residing on the HDD inside ACM. An ACM is a self-contained computing device that can be armed with security software and hardware to protect its owner's private files and data. ACM docks with a computer bay in a wide variety of peripheral consoles. The combined ACM and peripheral console function as a personal computer. A computer module interface bus connects ACM and peripheral device. In some embodiments, all ACM data passes through computer module interface (CMI) bus to reach any device in the peripheral console, i.e. floppy drive, removable media, secondary hard disk drive, modem, and others. CMI bus data transfer is controlled by a pair of interface controllers on either side of the bus. This partitioning of a personal computer offer a way of protecting against illegal access of data residing within ACM by guarding data transaction through the computer module interface bus.

In a specific embodiment, a secured ACM has an enclosure that includes the following components:

- 1) ACPU,
- 2) Main memory,
- 3) A primary Hard Disk Drive (HDD),
- 4) Operating System, application software, data files on primary HDD,
- 5) Interface circuitry and connectors to peripheral console,
- 6) Flash memory used for storing security code and ID,
- 7) Data detection and control circuitry to manage data flow to peripheral console,
- 8) Circuit board connecting the above components, and others.

A peripheral console includes some of the following elements:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. CRT monitor, or integrated LCD display,
- 3) Removable storage media subsystem, e.g. Floppy drive, CDROM drive,
- 4) Communication device, e.g. LAN or modem,
- 5) Computer Module Bay, interface device and connectors to ACM,
- 6) Flash memory with security ID,
- 7) Power supply or battery system, and other devices.

The Computer Module Bay (CMB) is an opening in a peripheral console that receives ACM. CMB provides mechanical protection and electrical connection to ACM. The Computer Module Interface bus is made up of 3 bus components: video bus, peripheral data bus, and power bus. Video Bus consists of video output of graphics devices, i.e. analog RGB and control signals for monitor, or digital video signals to drive flat panel displays. Power bus supplies the power for ACM. Peripheral data bus is a high speed, compressed,

8

peripheral bridge bus managed by a Host Interface Controller in ACM and a peripheral Interface Controller in peripheral console. In some embodiments, all peripheral data transaction passes through the interface controllers.

The implementation of the secured ACM generally includes the following elements:

- 1) A programmable Flash memory controlled by the Peripheral Interface Controller containing the security ID for the peripheral console,
- 2) A programmable Flash memory controlled by the Host Interface Controller containing hardware specific security code and ID for the computer module,
- 3) A data detection and control circuitry within Host Interface Controller to detect and manage data going out of ACM, and
- 4) A low level hardware dependent security code to perform security ID matching, hardware programming to manage data flow,
- 5) A high-level security program to manage user interface, program security ID, program security level, and other functions.

The hardware and software implementation allow more flexibility in the level of security protection offered to an ACM owner. Some examples of security levels are:

- 1) No access—Security IDs do not match according to owner's requirement. The Host Interface Controller blocks all peripheral data traffic between ACM and peripheral console except for keyboard and mouse,
- 2) Peripheral Read-only—No files can be written to any peripheral devices. All peripheral devices in peripheral console are managed as Read-only devices. The primary hard disk drive in ACM can be accessed freely,
- 3) Limited access—Certain peripheral devices are allowed read/write access, i.e. modem, and other devices are Read-only, i.e. removable media devices,
- 4) Full access—No restriction, and others.

Upon power up, the low level security code is executed to compare security ID between the respective flash memory between ACM and peripheral console. Typical security ID can include:

- 1) User ID
- 2) User password
- 3) User Access privilege
- 4) Business ID
- 5) Business password
- 6) Equipment ID
- 7) Equipment access privilege, and any other security IDs.

The user through the security program can activate different levels of password protection, which can be stored in a look up table. The company through the security program can control different levels of access privilege of a user, a business group, or equipment. The security code then program the security level allowed by the access privilege determined by the security ID matching result. For example, if an unidentified peripheral console is detected upon power up by the low level security code, e.g. a home unit, the access privilege can set to Peripheral Read-only. With Read-only access privilege for all peripheral devices in peripheral console, the data detection and control circuitry is programmed to monitor all data traffic going to the peripheral console. Any memory block transfer to peripheral console will be detected and blocked. Under this mode, a user can use the computer with free access to the primary HDD in ACM. Any files can be read from other storage media in the peripheral console. But no files from the primary HDD can be copied to another media.

The data detection circuitry separately monitors peripheral bus operation type and memory address range being

## US RE43,171 E

9

accessed. A specific address range for memory accesses and for I/O accesses can be programmed for the data detection circuitry to flag a match. A data blocking circuitry is triggered by the detection circuitry when a match occurs, and blank out the data that is being sent to the peripheral console. For the security system to be effective, a [temper] *tamper* resistant enclosure must be used to prevent removal of the hard disk drive and the flash memory inside ACM. Further details are shown throughout the present specification and more particularly below.

FIG. 4 is a simplified illustration of security systems 300 according to embodiments of the present invention. This illustration is merely an example, which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The systems show various examples of ways to implement the present invention. Here, a user relies upon certain consoles to access information. A company's shared portable console 325 can access general company information 303. Selected security identification information 315 is entered into the shared console to access the information via a network. The information generally includes owner, owner password, business, business password, console type, location, and access privilege information, which is displayed on a user display. The owner is generally the user name. Owner password is the user password. The business is the business unit name and business password is the business unit password. The console type can be portable for laptops, notebooks, and the like. Alternatively, the console type can be a desktop. The location generally specifies the desktop location or address for a networked system. Alternatively, the location can also be a home location. Access privilege can be categorized into many different levels. For example, the user can access general company information, but not information directed to other business units. The user can also be limited to access his/her private information, which is company related. Many other types of information can be restricted or accessed depending upon the embodiment.

Other types of access can be granted depending upon the consoles. For example, various consoles include, among others, a console at a user's home, e.g., "John Doe's," a console in the user's office 329, a console in a co-worker's office 331, which the user can access. The access from John Doe's home console uses security identification 317 and provides restricted access 305. The user's use of the module 307 can be from a variety of consoles and is accessed using security identification 319. Here, access privilege is private, which allows the user to access private personal information or private company information that the user has created. The user's access from his office relies upon security identification 321, which grants access to private information and general company information. The co-worker's console can also be used with security identification 323, which allows the user to access general company information but not private information of John Doe, for example. Depending upon the console used by the user, the security system can provide partial or full access to information on servers via network as well as an attached computer module. Information can also be limited to read only for certain information sources such as a server, a hard drive, a floppy drive, and others.

In a specific embodiment, the present invention also provides a security feature for the ACM 307. Here, the user of the ACM can be granted access to information in the ACM if the correct security identification information 319 is provided to the combination of ACM and console. Once the correct information is provided, the user can access the information on the

10

hard drive of the ACM, which can be for private use. Other levels of access and security can also be provided depending upon the application.

FIG. 5 is a simplified diagram 500 of a computer module in a console according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 500 includes an attached computer module 501 and a peripheral console 503, as well as other elements as desired. These elements have a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

The block diagram 500 illustrates attached computer module 501. The module 501 has a central processing unit 502, which communicates to a north bridge 541, by way of a CPU bus 527. The north bridge couples to main memory 523 via memory bus 529. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem 515 via bus 542. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive 509 that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines 502 and 531. The hard disk drive controller couples to the north bridge by way of the host PCI bus 531, which connects bus 537 to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device 505 with a BIOS. The flash memory device 505 also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 512 kilobits or greater of memory, or 1 megabits or greater of memory. The flash memory device can store a security identification number or the like. The flash memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The flash memory generally has at least 128 kilobits storage cells or more. The flash memory can be any product such as a W29C020 product made by a company called Winbond of Taiwan, but can also be others. The flash memory cell and user identification will be more fully described below in reference to the FIGS. A host interface controller 507 communicates to the north bridge via bus 535 and host PCI bus. The host interface controller also has a data control 511. Host interface controller 507 communicates to the console using bus 513, which couples to connection 515.

Peripheral console 503 includes a variety of elements to interface to the module 501, display 551, and network 553. The console forms around south bridge 571, which couples to



## US RE43,171 E

11

bus **563**, which couples to bus **561**. Bus **561** is in communication with network card **555**, which is a local area network for Ethernet, for example. South bridge also couples through control **569** to peripheral interface controller **567**, which also communicates to bus **561**. Peripheral interface controller also couples to host interface controller through connection **515** and bus **513**. The peripheral console has a primary removable drive **559** connected to south bridge through bus **575**. South bridge also couples to secondary hard disk through bus **577**.

In a specific embodiment, the peripheral console also has a serial EEPROM memory device **575**, which is coupled to the peripheral interface controller. The memory device can store a security identification number or the like. The memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The memory generally has at least 16 kilobits of storage cells or more. Preferably, the memory device is a 16 kilobit device or 64 megabit device or greater, depending upon the application. The memory can be any product such as a X24320 product made by a company called Xicor, but can also be others. The memory cell and user identification will be more fully described below in reference to the FIGS.

FIG. **6** is a simplified diagram of a security method **600** for a module according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The present method shows an example of how the present security method can be implemented. The present method uses a combination of software **601** and hardware **603**, which is in the computer module. A plurality of external devices can be accessed depending upon the embodiment. These external devices include a secondary hard drive **618**, a removable drive **619**, a network (e.g., LAN, modem) device **621**, and others. A keyboard **623** is also shown, which can act locally.

The software **601** includes an operating system **609**, application programs **607**, and a data security and initialization program **605**. Other programs can also exist. Additionally, some of these programs may not exist. Preferably, the data security and initialization program exists. This data security and initialization program is initiated once the attached computer module is inserted into the console. The program interface and oversees a variety of hardware features, which will be used to control access to the external devices, for example. Of course, the particular configuration of the software will depend upon the application.

Hardware features can be implemented using a primary hard disk **611** coupled to a CPU/cache combination, which includes a main memory. The main memory is often a volatile memory such as dynamic random access memory. Data from any one of the external devices can enter the CPU/cache combination. For example, the secondary hard disk memory and I/O address range data is transferred **624** to the CPU/cache combination. The removable drive memory and I/O address range data can also transfer **625** to the CPU/cache combination. The LAN memory and I/O address range data can also transfer **626** to the CPU/cache combination. Keyboard data can also transfer **627** to the CPU/cache combination. To write data from the module into any one of these external elements, the data security program interfaces with the data detection and control circuit to determine if such data should be transferred to any one of the external elements. As noted, the external elements include, among others, secondary hard disk, and removable drive. Here, the data security program checks the security identification number with other numbers to determine the security access level. There are

12

many other ways that the present invention can be implemented. These methods are described more fully below.

FIG. **7** is a simplified diagram **700** of a method according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The present method begins at power up, which is step **701**. The present method reads a security code, which has been entered by a user, for example, in step **703**. The security code can be a string of characters, including numbers and letters. The security code is preferably a mixture of numbers and letters, which are at least about 6 characters in length, but is not limited.

The present method reads (step **703**) the security code, which has been entered. Next, the security code is compared with a stored code, which is in flash memory or the like (step **705**). If the compared code matches with the stored code, the method resumes to step **708**. Alternatively, the method goes to step **707** via branch **706** where no access is granted. When no access is granted, all data are blocked out from the user that attempts to log onto the system. Alternatively, the method determines if a certain level of access is granted, step **708**. Depending upon the embodiment, the present method can grant full access, step **710**, via branch **716**. The present method allows full access based upon information stored in the flash memory device. Alternatively, the method can allow the user to access a limited amount of information.

Here, the present method allows for at least one or more than two levels of access. In a specific embodiment, the present method allows for the user of the module to access peripheral storage (step **711**). The access privilege is read-only. The user can read information on the peripheral storage including hard disks and the like. Once the user accesses the storage, the method data control, step **719**, takes over, where the hardware prevents the user from accessing other information, step **721**. In a specific embodiment, the method can allow information to be removed from the peripheral storage. If the method allows for data to be removed, step **723**, the method goes through branch **731** to let data out, which can occur through the module. Alternatively, the method goes to block data (step **725**) via branch **733**. Depending upon the embodiment, the method returns to the decision block, step **723**. Alternatively, the method traverses branch **714** to a peripheral read-only process, step **712**. The read-only process programs data control, step **713**. Next, the hardware takes over (step **715**). The method blocks all data from being accessed by the user, step **717**.

FIG. **8** is a simplified diagram of a system **800** according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The system **800** includes an attached computer module **801**, which can be inserted into one of a plurality of console devices to create a "plug and play" operation. For example, the console device can be peripheral console **801** or peripheral console **805**. Each peripheral console can have similar or different connection characteristics. Peripheral console **803** couples to a local area network using Ethernet **817**. Peripheral console **805** couples to a DSL line **827** through a DSL modem **825**. Other consoles can also be included to use other types of networks such as ADSL, Cable Modem, wireless, Token Ring, and the like.

As shown, the attached computer module has elements such as a memory region **807**, which stores BIOS information, a security code, and a security identification number on a flash memory device or the like. The memory region

## US RE43,171 E

13

couples to a central processing region **809**, which can include CPU, chipset, cache memory, graphics, and a hard disk drive, as well as other features. The central processing region couples to a host interface controller, which interfaces the attached computer module to one of the peripheral consoles. Any of the above information can also be included in the attached computer module.

Each peripheral console also has a variety of elements. These elements include a region **813**, **821**, which has a flash memory device with a security identification number, a password, access information, access privileges, internet service provider access information, as well as other features, which were previously noted. The peripheral console also has an interface controller **815**, **823**, which couples region **813**, **821**, respectively to a networking device **817**, **825**. The networking device can be an Ethernet card **817**, which allows communication to the local area network **819**. Alternatively, the networking device can be a DSL modem **825**, which allows communication to a DSL (or ADSL) phone line. Other types of networking device can also be used, depending upon the application.

Each console provides a selected connection based upon set of predefined factors. These factors include communication hardware information so that software in attached computer module can read and allow a connection to a network. Here, access information can be provided to the user. Information about connection information will also be included. This connection information includes telephone numbers, account numbers, passwords (local), or a company password. The console and module combination will take care of charges, etc. based upon time bases. Module will have credit card information, but will have security. In a specific embodiment, the module inserts into the console. The module then asks the console which hardware will be used. If the hardware is an Ethernet connect, the module configures connection information to access the Ethernet connection. Alternatively, if the hardware requires a DSL connection, the module configures connection information to access the DSL connection. Other configuration information such as company server information, password, can also be provided.

*Embodiments in accordance with the present invention may interface two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In accordance with embodiments of the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.*

*The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using low voltage differential signal (LVDS) channels for the interface. An LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. An interface having a smaller number of signal channels and, therefore, a*

14

*smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.*

*In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operate. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the host interface controller (HIC) to the peripheral interface controller (PIC) while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.*

*FIG. 9 is a block diagram of one embodiment of a computer system 900 using the interface of the present invention. Computer system 900 includes an ACM 905 and a peripheral console 910, which are described in greater detail in the application of William W. Y. Chu for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998, now U.S. Pat. No. 6,216,185, and incorporated herein by reference. The ACM 905 and the peripheral console 910 are interfaced through an exchange interface system (XIS) bus 915. The XIS bus 915 includes power bus 916, video bus 917 and peripheral bus (XPBus) 918, which is also herein referred to as an interface channel. The power bus 916 transmits power between ACM 905 and peripheral console 910. In a preferred embodiment power bus 916 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 917 transmits video signals between the ACM 905 and the peripheral console 910. In a preferred embodiment, the video bus 917 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-Video) signals. The XPBus 918 is coupled to host interface controller (HIC) 919 and to peripheral interface controller (PIC) 920, which is also sometimes referred to as a bay interface controller. In the embodiment shown in FIG. 9, HIC 919 is coupled to an integrated unit 921 that includes a CPU, a cache and a north bridge.*

*FIG. 10 is a detailed block diagram of one embodiment of the host interface controller (HIC) of the present invention. As shown in FIG. 10, HIC 1000 comprises bus controller 1010, translator 1020, transmitter 1030, receiver 1040, a PLL 1050, an address/data multiplexer (A/D MUX) 1060, a read/write controller (RD/WR Cntl) 1070, a video serial to parallel converter 1080 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1090.*

*HIC 1000 is coupled to an optional flash memory BIOS configuration unit 1001. Flash memory unit 1001 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1060 and RD/WR Control 1070, which control the programming, read, and write of flash memory unit 1001.*

*Bus controller 1010 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1010 includes a slave (target) unit 1011 and a master unit 1016. Both slave unit 1011 and master unit 1016 each include two first in first out (FIFO) buffers, which are preferably*

## US RE43,171 E

15

asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1016 as well as the two FIFOs in the slave unit 1011 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1011 includes encoder 1022 and decoder 1023, while master unit 1016 includes encoder 1027 and decoder 1028. The FIFOs 1012, 1013, 1017 and 1018 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 10 operate at 33 MHz and 66 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1023 and 1028 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 1013 and 1018 prior to being transferred to the host PCI bus. FIFOs 1012, 1013, 1017 and 1018, allow bus controller 1010 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

Bus controller 1010 also comprises slave read/write control (RD/WR Cntl) 1014 and master read/write control (RD/WR Cntl) 1015. RD/WR controls 1014 and 1015 are involved in the transfer of PCI control signals between bus controller 1010 and the host PCI bus.

Bus controller 1010 is coupled to translator 1020. Translator 1020 comprises encoders 1022 and 1027, decoders 1023 and 1028, control decoder & separate data path unit 1024 and control encoder & merge data path unit 1025. As discussed above encoders 1022 and 1027 are part of slave data unit 1011 and master data unit 1016, respectively, receive PCI address and data information from FIFOs 1012 and 1017, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders 1023 and 1028 are part of slave data unit 1011 and master data unit 1016, respectively, and format address and data information from receiver 1040 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 1025 receives PCI control signals from the slave RD/WR control 1014 and master RD/WR control 1015. Additionally, control encoder & merge data path unit 1025 receives control signals from CPU CNTL & GPIO latch/driver 1090, which is coupled to the CPU and north bridge (not shown in FIG. 10). Control encoder & merge data path unit 1025 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 1030, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit 1024 receives control bits from receiver 1040 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit 1024 separates the control bits it receives from receiver 1040 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

16

Transmitter 1030 receives multiplexed parallel address/data (A/D) bits and control bits from translator 1020 on the AD[31:0] out and the CNTL out lines, respectively. Transmitter 1030 also receives a clock signal from PLL 1050. PLL 1050 takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 66 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 66 MHz rather than 33 MHz or having 64 rather than 32 multiplexed address/data lines.

The multiplexed parallel A/D bits and some control bits input to transmitter 1030 are serialized by parallel to serial converters 1032 of transmitter 1030 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 1033 into 10 bit packets and send out on control line PCN of the XPBus.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 11, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

FIG. 12 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1200 is nearly identical to HIC 600 in its function, except that HIC 600 interfaces the host PCI bus to the XPBus while PIC 1200 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 1200 serve the same function as their corresponding components in HIC 600. Reference numbers for components in PIC 1200 have been selected such that a component in PIC 1200 and its corresponding component in HIC 600 have reference numbers that differ by 500 and have the same two least significant digits. Thus for example, the bus controller in PIC 1200 is referenced as bus controller 1210 while the bus controller in HIC 600 is referenced as bus controller 610. As many of the elements in PIC 1200 serve the same functions as those served by their corresponding elements in HIC 600 and as the functions of the corresponding elements in HIC 600 have been described in detail above, the function of elements of PIC 1200 having corresponding elements in HIC 600 will not be further described herein. Reference may be made to the



## US RE43,171 E

17

above description of FIG. 6 for an understanding of the functions of the elements of PIC 1200 having corresponding elements in HIC 600.

As suggested above, there are also differences between HIC 600 and PIC 1200. Some of the differences between HIC 600 and PIC 1100 include the following. First, receiver 1240 in PIC 1200, unlike receiver 640 in HIC 600, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 600 synchronizes the PCKR clock to the PCK clock locally generated by PLL 650. PIC 1100 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 600. Another difference between PIC 1200 and HIC 600 is the fact that PIC 1200 contains a video parallel to serial converter 1289 whereas HIC 600 contains a video serial to parallel converter 680. Video parallel to serial converter 1289 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0:15] and Video Port Control lines, respectively, from the video capture circuit (not shown in FIG. 12) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC 1200, unlike HIC 600, contains a clock doubler 1282 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1282 through buffer 1283 and is sent to serial to parallel converter 680 through buffer 1284. Additionally, reset control unit 1235 in PIC 1200 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1190 and transmits the reset signal on the RESET# line to the HIC 600 whereas reset control unit 645 of HIC 600 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 690 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1200 to the HIC 600.

The XPBUS which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBUS, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

In the embodiment shown in FIG. 9, HIC 919 is coupled to an integrated unit 921 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 13, the CPU 1305 and north bridge 1310 are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 14, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 1405 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1410 includes a PIC and a south bridge.

Although the functionality above has been generally described in terms of a specific sequence of steps, other steps can also be used. Here, the steps can be implemented in a combination of hardware, firmware, and software. Either of these can be further combined or even separated. Depending

18

upon the embodiment, the functionality can be implemented in a number of different ways without departing from the spirit and scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

[1. A security protection method for a computer module, said method comprising:

inserting the computer module into a console;  
initiating a security program in said module to read a security identification of said console and to read a security identification of said computer module;  
determining of a predetermined security status based upon a relationship of said console identification and said computer module identification;  
selecting said predetermined security status; and  
operating said computer module based upon said security status.]

[2. The method of claim 1 wherein said predetermined security status disables a network access to the computer module.]

[3. The method of claim 1 wherein said predetermined security status disables a secondary storage of information from said computer module to substantially prevent information to be transferred from a memory of the computer module to said secondary storage.]

[4. The method of claim 1 wherein said security program is provided in a system BIOS.]

[5. The method of claim 1 wherein said step of initiating reads said security identification of said computer module from a flash memory device.]

[6. The method of claim 1 wherein said step of initiating reads said security identification of said console from a flash memory device.]

[7. The method of claim 1 wherein said console is selected from a desktop home computing device, an office desktop computing device, a mobile computing device, a television set-top computing device, and a co-worker's computing device.]

[8. A system for secured information transactions, the system comprising:

a console comprising a peripheral controller housed in the console;  
a user identification input device coupled to the peripheral controller, the user identification input device being provided for user identification data; and  
an attached computer module coupled to the console, the attached computer module comprising a security memory device stored with the user identification data.]

[9. The system of claim 8 wherein the user identification input device is a finger print reader.]

[10. The system of claim 8 wherein the user identification input device is a voice processing device.]

[11. A method for operating a module computer into one of a plurality of network systems, the method comprising:

providing a computer module, the module comprising a connection program;  
inserting the computer module into a computer console, the computer console having access to a network;  
receiving connection information from the computer console;

## US RE43,171 E

19

configuring the connection program to adapt to the connection information; and  
establish a connection between the computer module and a server coupled to the network.]

[12. The method of claim 11 wherein the connection information comprises a connection protocol for providing the connection.]

[13. The method of claim 12 wherein the connection protocol is selected from TCP/IP, or mobile IP.]

14. A system for secured information transactions, the system comprising:

a console comprising a network controller housed in the console;

a user identification input device coupled to the network controller; and

an attached computer module coupled to the console, the attached computer module comprising

a central processing unit,

a device stored with a user identification data,

a security program providing password protection for access to the computer module based on the user identification data,

an integrated interface controller and bridge unit to communicate an encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction, the integrated interface controller and bridge unit directly coupled to the central processing unit, and

a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction,

wherein the low voltage differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

15. The system of claim 14 wherein the encoded serial bit stream comprises 10 bit packets.

16. The system of claim 14 wherein the integrated interface controller and bridge unit is coupled to the central processing unit without any intervening PCI bus.

17. The system of claim 16 wherein the integrated interface controller and bridge unit comprises a north bridge and an interface controller integrated with the north bridge, and the low voltage differential signal channel extends from the interface controller to convey the encoded serial bit stream of PCI bus transaction.

18. The system of claim 16 further comprising a peripheral component coupled to the central processing unit through the low voltage differential signal channel.

19. The system of claim 16 wherein the attached computer module further comprises a main memory coupled to the central processing unit through the integrated interface controller and bridge unit.

20. The system of claim 16 wherein the integrated interface controller and bridge unit is configured to output encoded PCI address and data bits in serial form that are conveyed over the low voltage differential signal channel.

21. The system of claim 16 wherein the encoded serial bit stream of PCI bus transaction comprises information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel.

22. The system of claim 16 wherein the low voltage differential signal channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

20

23. The system of claim 16 wherein the network controller comprises an Ethernet controller.

24. A method comprising:

providing a computer module, the module comprising a central processing unit,

a connection program,

an integrated interface controller and bridge unit to output an encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction, the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus, and

a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction;

inserting the computer module into a computer console, the computer console having access to a network;

receiving connection information from the computer console;

configuring the connection program to adapt to the connection information; and

establishing a connection between the computer module and a server coupled to the network,

wherein the low voltage differential signal channel further comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

25. The method of claim 24 wherein the connection between the computer module and the server comprises an Ethernet connection.

26. The method of claim 24 wherein the connection protocol is TCP/IP.

27. The method of claim 24 further comprising conveying, over the low voltage differential signal channel, the encoded serial bit stream of PCI bus transaction as 10 bit packets.

28. The method of claim 27 wherein conveying the encoded serial bit stream of PCI bus transaction comprises conveying information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel.

29. A system of connecting a computer module to a network, the system comprising:

a console having access to a network;

a computer module inserted into the console and powered by the console, the computer module comprising a central processing unit,

a peripheral bridge coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, the peripheral bridge comprising an interface controller to communicate an encoded serial bit stream of address and data bits of PCI bus transaction,

a low voltage differential signal channel extending from the interface controller to convey the encoded serial bit stream of PCI bus transaction, and

a connection program receiving connection information from the console, configuring the connection program to adapt to the connection information, and establishing a connection between the computer module and a server coupled to the network,

wherein the low voltage differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

30. The system of claim 29 wherein the encoded serial bit stream comprises 10 bit packets.

31. The system of claim 29 wherein the interface controller is integrated with the peripheral bridge as a single integrated unit.



## US RE43,171 E

## 21

32. The system of claim 31 wherein the peripheral bridge comprises a north bridge.

33. The system of claim 32 further comprising a south bridge coupled to the north bridge through the low voltage differential signal channel.

34. The system of claim 31 wherein the interface controller is coupled to the central processing unit without any intervening PCI bus.

35. The system of claim 31 wherein each of the unidirectional serial bit channels corresponds to a point-to-point link.

36. A system for secured information transactions, the system comprising:

a console comprising a network communication controller housed in the console;

a user identification input device coupled to the console, the user identification input device being provided for user identification data; and

an attached computer module coupled to the console, the attached computer module comprising

a central processing unit,

a security program,

a peripheral bridge directly coupled to the central processing unit, the peripheral bridge comprising an interface controller, the peripheral bridge and the interface controller configured as a single integrated unit, and

a low voltage differential signal channel that comprises two sets of unidirectional serial bit channels in opposite directions which transmit data in 10 bit packets, the low voltage differential signal channel coupled to the interface controller;

wherein said security program receives the user identification data from the console, determines a predetermined security status, and operating said computer module based upon said security status.

37. The system of claim 36 wherein the data packets comprise an encoded bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction.

38. The system of claim 37 wherein the interface controller is configured to transmit and receive encoded PCI address and data bits over the low voltage differential signal channel.

39. The system of claim 38 wherein the interface controller is coupled to the central processing unit without any intervening PCI bus.

40. The system of claim 38 wherein the peripheral bridge comprises a north bridge.

41. The system of claim 40 further comprising a south bridge coupled to the north bridge.

42. The system of claim 41 wherein the south bridge is coupled to the north bridge through the low voltage differential signal channel.

43. The system of claim 38 wherein the low voltage differential signal channel comprises two sets of unidirectional, multiple serial bit channels to convey data in opposite directions, and each of the unidirectional, multiple serial bit channels corresponds to a point-to-point link.

44. A system for secured information transactions, the system comprising:

a computer console comprising

a network communication controller housed in the console,

a low voltage differential signal (LVDS) channel comprising two sets of multiple unidirectional serial channels that transmit encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in opposite directions, and

## 22

a user identification input device coupled to the console, the user identification input device being provided for user identification data; and

an attached computer module that inserts into the console in a "plug and play" operation, the attached computer module comprising

a security program providing password protection for data content within said attached computer module,

a security memory device stored with the user identification data, and

an interface controller coupled to the console through serial bit based lines;

wherein the interface controller transfers data between the computer module and the console in Universal Serial Bus (USB) protocol.

45. The system of claim 44 wherein said attached computer module inserts into the console and is powered by the console to form a functional computer.

46. The system of claim 44 wherein the attached computer module has a tamper resistant enclosure.

47. The system of claim 44 wherein the security memory device comprises of flash memory.

48. The system of claim 44 wherein the console further comprises an integrated interface controller and bridge unit to transmit and receive encoded serial bits of PCI bus transaction over the LVDS channel.

49. The system of claim 48 wherein the encoded serial bits of PCI bus transaction comprise information to permit decoding to create a PCI bus transaction.

50. A system for secured information transactions, the system comprising:

a console comprising a network communication controller housed in the console;

a user input device coupled to the console, the user input device being provided for user identification data; and

an attached computer module inserted into the console, the attached computer module comprising

a central processing unit,

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, the peripheral bridge comprising an integrated interface controller to communicate an encoded serial bit stream of address and data bits of PCI bus transaction,

a low voltage differential signal channel extending from the integrated interface controller to convey the encoded serial bit stream of PCI bus transaction, and a mass storage unit storing a security program and user identification data;

wherein the security program receives the user identification data from the input device, matches the stored user identification data and permits external access to the computer module,

wherein the low voltage differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions, and each of the unidirectional serial bit channels corresponds to a point-to-point link.

51. The system of claim 50 wherein the security program further determines a predetermined security status, and controls different levels of access privilege to said attached computer module.

52. The system of claim 50 wherein the encoded serial bit stream comprises 10 bit packets.

53. The system of claim 50 wherein the peripheral bridge comprises a north bridge.

## US RE43,171 E

23

54. The system of claim 50 wherein the integrated interface controller is coupled to the central processing unit without any intervening PCI bus, and the integrated interface controller is configured to output encoded address and data bits of PCI bus transaction in serial form that are conveyed over the low voltage differential signal channel.

55. The system of claim 50 wherein the low voltage differential signal channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

56. A system comprising:

a console housing a network controller and a low voltage differential signal serial channel for communicating encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction;

a user identification input device coupled to the console; and

an attached computer module coupled to the console, the attached computer module comprising  
a device stored with a user identification data,  
a security program providing protection for access to the computer module based on the user identification data, and  
an interface controller coupled to the console for communicating data in a serial bit stream,

wherein the low voltage differential signal serial channel further comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

57. The system of claim 56 wherein the encoded address and data bits of PCI bus transaction comprise 10 bit data packets.

58. The system of claim 56 wherein the computer module further comprises a flash memory mass storage device.

59. The system of claim 56 wherein the serial bit stream transmits data packets in Universal Serial Bus (USB) protocol.

60. A system for secured information transactions, the system comprising:

a console comprising a peripheral controller housed in the console;

a user identification input device coupled to the peripheral controller, the user identification input device being provided for user identification data; and

24

an attached computer module coupled to the console, the attached computer module comprising  
a security memory device stored with the user identification data,

a central processing unit,

an integrated interface controller and bridge unit to communicate an encoded serial stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction as 10 bit packets, the integrated interface controller and bridge unit directly coupled to the central processing unit, and

a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial stream of PCI bus transaction, the low voltage differential signal channel comprising two sets of unidirectional serial bit channels which transmit data in opposite directions.

61. The system of claim 60 wherein the integrated interface controller and bridge unit is coupled to the central processing unit without any intervening PCI bus.

62. The system of claim 61 wherein the integrated interface controller and bridge unit comprises a north bridge and an interface controller integrated with the north bridge, and the low voltage differential signal channel extends from the interface controller to convey the encoded serial stream of PCI bus transaction.

63. The system of claim 61 wherein the attached computer module further comprises a main memory coupled to the central processing unit through the integrated interface controller and bridge unit.

64. The system of claim 61 wherein the integrated interface controller and bridge unit is configured to output encoded PCI address and data bits in serial form that are conveyed over the low voltage differential signal channel.

65. The system of claim 61 wherein the encoded serial stream of PCI bus transaction comprises information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel.

66. The system of claim 61 wherein the low voltage differential signal channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

\* \* \* \* \*